File 2:INSPEC 1969-2002/May W3


| Set | Items | Description |
|---|---|---|
| S1 | 317 | FLUOROCARBONS |
| S2 | 5152 | CI=NH3 BIN |
| S3 | 2 | S1 AND (S2 OR AMMONIA) |

3/3,AB/1
DIALOG(R)File 2:INSPEC


5501769 INSPEC Abstract Number: B9703-0170J-101
Title: Residual gas analysis as a failure analysis tool for microelectronic devices
Author(s): Kumar, A.; Carreon, M.
Author Affiliation: SEAL Lab., El Segundo, CA, USA
Conference Title: Wescon/96 Conference Proceedings (Cat. No.96CH35927) p.114-15
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA ix+682 pp.
ISBN: 0 7803 3274 1 Material Identity Number: XX96-03301
Conference Title: Wescon/96
Conference Sponsor: Los Angeles and San Francisco Bay Area Councils, IEEE ; Southern & Northern California Chapters, ERA
Conference Date: 22-24 Oct. 1996 Conference Location: Anaheim, CA, USA
Language: English
Abstract: Moisture measurement is the most important information obtained during the residual gas analysis (RGA) of microelectronic packages containing cavities. The MIL-STD-883, Method 1018.2 specification has a moisture requirement of 5000 ppmv maximum. In addition to moisture analysis during RGA, several other gases are also analyzed; most common gaseous species analyzed are nitrogen oxygen, carbon dioxide, hydrogen, argon, helium, **fluorocarbons**, methane, and **ammonia**. Based on this, conclusions can be made regarding the internal atmosphere, sources of moisture, hermeticity of the package, outgassing from the die attach epoxy material or other organic materials, etc., during failure analysis of devices that fail to meet the moisture requirements or do not reflect the anticipated gas composition.
Subfile: B


3/3,AB/2
DIALOG(R)File 2:INSPEC


01696185 INSPEC Abstract Number: B81031068
Title: Condenser designs for binary power cycles
Author(s): Michel, J.W.; Murphy, R.W.
Author Affiliation: Energy Div., Oak Ridge Nat. Lab., Oak Ridge, TN, USA

Conference Title: "Energy to the 21st Century". Proceedings of the 15th Intersociety Energy Conversion Engineering Conference p.449-54
Publisher: AIAA, New York, NY, USA
Publication Date: 1980 Country of Publication: USA 3 vol. xxii+2669 pp.
Conference Sponsor: ASME; AIAA; IEEE; et al
Conference Date: 18-22 Aug. 1980 Conference Location: Seattle, WA, USA
Language: English
Abstract: For the past four years, work has been in progress at ORNL to develop improved condensers for geothermal binary power cycles. The work has centered on optimizing the design variables associated with fluted surfaces on vertical tubes and comparing the tube performance with available enhanced tubes either for vertical or horizontal operation. Data with seven fluids including a hydrocarbon, **fluorocarbons**, and

**ammonia** condensing on up to 30 different tubes have been obtained. Data for tubes of different effective lengths (0.15 to 1.20 m) and inclination have also been obtained. The primary conclusion from this work is that fluted tubes can provide an enhancement in condensation coefficient of a factor of 6 over smooth vertical tubes and a factor of 2 over enhanced commercial tubes either operating vertically or horizontally. These data, together with field test data, have formed the basis for designing two prototype condensers, one for the 60 kWe Raft River, Idaho, Pilot plant and one for the 500 kWe East Mesa, California, direct-contact demonstration plant.

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     FILE 'WPIX, JAPIO' ENTERED AT 12:01:43 ON 24 MAY 2002
L1        18227 S C4F8 OR C4F6 OR C5F8 OR CF4 OR C2F6 OR C3F8 OR FLUOROCARBON O
L2        79604 S NH3 OR AMMONIA
L3          268 S L1 AND L2
L4           55 S L3 AND (DIELECTRIC OR INSULAT? OR OXIDE)(3N)(LAYER OR FILM OR
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DNN N2002-137758 DNC C2002-056451
TI Semiconductor device manufacture involves etching nitriding film using mixture of carbon and fluorine gas.
DC L03 U11 V05
PA (NIDE) NEC CORP
CYC 1
PI JP 2001127039 A 20010511 (200224)* 5p
ADT JP 2001127039 A JP 1999-302329 19991025
PRAI JP 1999-302329 19991025
AB JP2001127039 A UPAB: 20020416
NOVELTY - A nitride film (4) is formed covering a polysilicon gate (2) and WSi (3) which are formed on a substrate (1): An **oxide film** (5) that is provided on nitride film is etched to form a vent by using mixed gas. Then nitriding film is etched by using CxFy gas.
DETAILED DESCRIPTION - The CxFy mixed gas is chosen among the gases of C3F6, **C4F6**, **C4F8**, **C5F8**, CH2F2, CH3F, CH3 or Br gas, **NH3** gas, C2H5OH, CH3OH or its additions.
USE - Manufacture of semiconductor device.
ADVANTAGE - Since etching gas group of interlayer **oxide film** is used for nitriding film etching, sufficient etching is done without changing atmosphere of etching chamber.
DESCRIPTION OF DRAWING(S) - The figure shows section of manufacture of semiconductor device. (Drawing includes non-English language text).
Substrate 1
Polysilicon gate 2
WSi 3
Nitride film 4
**Oxide film** 5
Dwg.1/2

L4 ANSWER 6 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2002-171742 [22] WPIX
DNN N2002-130567 DNC C2002-053170
TI Producing a gate for a CMOS transistor structure having channel of reduced length involves treatment of etching deposit formed during anisotropic etching of gate material to form protective layer against isotropic etching of gate material.
DC L03 U11 U13
IN MIZUSHIMA, K
PA (SHHA) SHINETSU HANDOTAI CO LTD
CYC 23
PI WO 2002005337 A1 20020117 (200222)* JA 35p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: JP KR SG US
ADT WO 2002005337 A1 WO 2001-JP5888 20010706
PRAI JP 2000-208459 20000710
AB WO 200205337 A UPAB: 20020409
NOVELTY - Unmasked gate material is anisotropically etched to its lower part, and an etching deposit formed on the sides of the etching is treated to form a protective layer against subsequent etching of the gate material. Gate material lower part is then isotropically etched down to a gate **insulating layer** (41) such that the gate (49) has a shorter width at its base.
DETAILED DESCRIPTION - A gate (49) for a CMOS transistor structure whose gate length is smaller at the bottom of the gate than at the top of the gate is produced from a stack comprising, in succession, a gate **insulating layer** (41), a gate material layer and a gate mask.
The process involves:

(a) anisotropic etching of the upper part of the gate material that is not masked by the gate mask, allowing the lower part of the gate material layer to remain and producing a deposit of etching products on the side of the etchings;

(b) treating the deposit of etching products in order to form a protective layer against a subsequent etching process; and

(c) isotropic etching of the lower part of the gate material layer as far as the gate **insulating layer** (41), in order to provide the gate (49) with a width that is shorter at its bottom than at its top.

INDEPENDENT CLAIMS are given for use of the above process to produce:

(A) a silicon-based gate; and

(B) a metallic gate, where the gate material comprises an upper layer of semiconductor material and a lower layer of metallic material.

USE - CMOS transistor manufacture.

ADVANTAGE - The passivation layer formed during etching is used to provide the gate with an anisotropic etching profile at its top and a very largely isotropic profile at its bottom.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a CMOS transistor structure according to the invention.

Silicon substrate 40

Gate **insulating layer** 41

Etching plasma 48

Gate 49

Dwg.5/5

L4 ANSWER 7 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2002-146687 [19] WPIX
DNN N2002-111152 DNC C2002-045422
TI Fabrication of self-aligned borderless contact involves using dual damascene process having two etch-stop **layers** formed on respective **dielectric layers**.
DC L03 U11
IN LEE, Y; SHIH, C; WU, J
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6323118 B1 20011127 (200219)* 8p
ADT US 6323118 B1 US 1998-114129 19980713
PRAI US 1998-114129 19980713
AB US 6323118 B UPAB: 20020321

NOVELTY - A self-aligned borderless contact is fabricated by using a dual damascene process. Two etch-stop layers are formed on respective **dielectric layers**. A metal line trench pattern formed from patterning a second photoresist layer is etched into etch-stop **layers** forming opening and **dielectric layers** reaching a substructure to form the self-aligned contact.

DETAILED DESCRIPTION - Fabrication of a self-aligned borderless dual damascene contact comprises:

(i) providing a substrate (110) having a substructural and sequentially forming first **dielectric layer**, a first etch-stop **layer**, second **dielectric layer**, second etch-stop layer, and first photoresist layer.

(ii) The substructural has a semiconductor device within the substrate and an interconnect metal line formed on the substrate.

(iii) The first photoresist layer is patterned with contact/via hole.

(iv) The contact/via hole pattern is etched and an opening is formed in the second etch-stop layer.

(v) The contact hole pattern is disposed on the device in the substructure and the via hole pattern is disposed over the metal line in

the substrate.

(vi) The first photoresist layer is removed from the substrate and a second photoresist layer (170) is formed on the substrate.

(vii) The second photoresist layer is pattern with a metal line trench pattern (175').

(viii) The line trench pattern in the second photoresist layer is etched into underlying the substrate until etch-stop layers (130, 150) are reached.

(ix) The line trench pattern in the two etch-stop layers forming the line trench opening (175) into the etch-stop layers.

(x) The line trench pattern is etched into underlying substrate until the substructure is reached to complete the fabrication of the borderless contact.

(xi) The second photoresist layer is removed and metal in the contact/via opening in the **dielectric layers** (120, 140) is formed.

(xii) The excess metal is removed from the surface of the substrate in preparation for the complete fabrication of a semiconductor substrate using the dual damascene process.

USE - For fabricating self-aligned borderless dual damascene contact useful for ultra large scale integrated circuit chips.

ADVANTAGE - The self-aligned contact has a relaxed photolithographic alignment tolerances by using the modified dual damascene process having two etch-stop layers.

DESCRIPTION OF DRAWING(S) - The figure shows the etching of the second pattern into the **dielectric layers**.

Substrate 110

**Dielectric layers** 120, 140

Etch-stop layers 130, 150

Second photoresist layer 170

Line trench opening 175

Metal line trench pattern 175'

Dwg.3j/3

L4 ANSWER 8 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2002-040407 [05] WPIX
DNN N2002-029890 DNC C2002-011477
TI Cleaning of semiconductor structure by introducing inert gas to region, forming plasma, applying power to plasma, introducing reducing gas to plasma and reacting it with oxide, and reducing the power applied to plasma.
DC L03 U11
IN ALLEN, R D; KHOSLA, M; KLAWUHN, E; POWELL, R A; ROZBICKI, R T; SETTLES, E D; TAM, L
PA (NOVE-N) NOVELLUS SYSTEMS INC
CYC 1
PI US 6319842 B1 20011120 (200205)* 8p
ADT US 6319842 B1 US 2001-753432 20010102
PRAI US 2001-753432 20010102
AB US 6319842 B UPAB: 20020123

NOVELTY - Semiconductor structure is cleaned by introducing an inert gas to a region adjacent to the structure, forming a plasma to ionize the inert gas, applying power to the plasma at a higher level, introducing a reducing gas to the plasma, reducing the power applied to the plasma to a lower level, and allowing the educing gas to react with an oxide in the semiconductor structure.

DETAILED DESCRIPTION - Cleaning of semiconductor structure (20) involves introducing an inert gas to a region adjacent to the structure, forming a plasma to ionize the inert gas, applying power to the plasma at

a higher level set such that ions of the inert gas collide with the semiconductor structure to dislodge atoms of a contaminant from a surface of the structure, introducing a reducing gas to the plasma, reducing the power applied to the plasma to a lower level such that the ions of the inert gas do not have energy to cause atoms of the contaminant to be dislodged from the structure, and allowing the reducing gas to react with an oxide in the semiconductor structure.

USE - The process is used for cleaning a semiconductor structure to remove contaminants that could impair the operation of the semiconductor device.

ADVANTAGE - The process minimizes undue damage (e.g. faceting at the upper corners of the via) to the structure, and reduces the amount of copper deposited or the amount of contamination that deposits on the sidewalls of the via by shortening the sputtering time to that required to remove the non-volatile contaminants.

DESCRIPTION OF DRAWING(S) - The figures show first and second stages of the inventive process.

Semiconductor structure 20

Via 32

2A, 2B/5

L4 ANSWER 9 OF 55 WPIX (C) 2002 THOMSON DERWENT

AN 2001-624313 [72] WPIX

DNN N2001-465122 DNC C2001-186136

TI Fabrication method of electronic device on semiconductor substrate, involves forming and patterning **dielectric layer** on conductive gate structure formed on substrate, and subjecting substrate to preset plasma.

DC L03 U11

IN SMITH, P B

PA (TEXI) TEXAS INSTR INC

CYC 1

PI US 6277733 B1 20010821 (200172)* 9p

ADT US 6277733 B1 Provisional US 1998-103047P 19981005, US 1999-408022 19990929

PRAI US 1998-103047P 19981005; US 1999-408022 19990929

AB US 6277733 B UPAB: 20011206

NOVELTY - An electronic device is fabricated on a semiconductor substrate (402), by forming a conductive gate structure (412) containing oxygen-sensitive conductor, over a substrate. A **dielectric layer** (414) is formed and patterned on the substrate. The substrate is subjected to a combination of an active oxygen-free, hydrogen-containing, deuterium or deuterium-containing plasma which contains a **fluorocarbon** gas.

DETAILED DESCRIPTION - An electronic device is fabricated on a semiconductor substrate, by forming a conductive structure over a substrate. The conductive structure comprises an oxygen-sensitive conductor capable of being oxidized when contacted with oxygen. A **dielectric layer** is formed and patterned on the substrate in which the conductive structure is exposed. The substrate is then subjected to a combination of an active oxygen-free, hydrogen-containing, deuterium or deuterium-containing plasma which contains a **fluorocarbon** gas. Patterning of the **dielectric layer** is performed by forming a photoresist **layer** on the **dielectric** material **layer**, patterning and removing the photoresist layer. The photoresist layer is removed by subjecting the substrate to a plasma containing **ammonia** , hydride of nitrogen (N2H2), hydrogen sulfide, methane or deuteriated gases. Any exposed hydrocarbons formed over the semiconductor substrate,

are removed by subjecting the substrate to plasma. Subjecting the substrate to plasma does not substantially remove any exposed nitride-containing structures.

USE - For fabrication of electronic devices such as metal interconnects, metal lines, metal gates, memory devices, logic devices, power devices and microprocessors.

ADVANTAGE - The residues present on the metallic structure, exposed portions of **dielectric layer** surface and side walls of the vias of the **dielectric layer**, are removed efficiently.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of the semiconductor device.

Semiconductor substrate 402

Conductive gate structure 412

**Dielectric layer** 414

Dwg.2h/2

L4 ANSWER 10 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2001-566896 [64] WPIX
DNC C2001-168374
TI Formation of fluorine-containing thin film for optical device, by positioning target and substrate in vessel, supplying sputtering gas and fluorine-containing gas into vessel, and supplying power between target and anode.
DC M13
IN ANDO, K; BIRO, R; KANAZAWA, H; OTANI, M; SHINGU, T; SUZUKI, Y
PA (CANO) CANON KK; (ANDO-I) ANDO K; (BIRO-I) BIRO R; (KANA-I) KANAZAWA H; (OTAN-I) OTANI M; (SHIN-I) SHINGU T; (SUZU-I) SUZUKI Y
CYC 28
PI EP 1134303 A1 20010919 (200164)* EN 32p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
US 2001031543 A1 20011018 (200166)
JP 2002047565 A 20020215 (200215) 20p
ADT EP 1134303 A1 EP 2001-106040 20010312; US 2001031543 A1 US 2001-804266 20010313; JP 2002047565 A JP 2001-70555 20010313
PRAI JP 2000-153245 20000524; JP 2000-68513 20000313
AB EP 1134303 A UPAB: 20011105
NOVELTY - A fluorine-containing thin film is formed on a substrate by providing a vessel, positioning a target and the substrate inside the vessel, supplying a sputtering gas and a fluorine-containing gas into the vessel, and supplying a power between the target and an anode.

DETAILED DESCRIPTION - Formation of a fluorine-containing thin film on a substrate (70), involves

a) providing a vessel (10);

b) placing a target (13) such that a target surface to be sputtered surrounds a discharge space (18);

c) placing the substrate on a side of an opening of the discharge space such that the substrate faces an anode (41) disposed to close another opening of the discharge space surrounded by the target;

d) supplying a sputtering gas (30) and a fluorine-containing gas (31) into the vessel; and

e) supplying a direct current (DC) power (80), or a power obtained by superimposing pulses with reversing polarities on the DC power, between the target and the anode, in which a discharge is induced in the discharge space to sputter the target.

An INDEPENDENT CLAIM is also included for an optical device including an optical system having an optical part made by forming a fluorine-containing thin film on a substrate by the invented process, in

combination with a laser light source for generating an ultraviolet light.

USE - For forming fluorine-containing thin film used for optical device. Preferably, the fluorine-containing thin film is a film of magnesium fluoride, aluminum fluoride, lanthanum fluoride, neodymium fluoride, thorium fluoride, lithium fluoride, yttrium fluoride, calcium fluoride, or gadolinium fluoride. It can also be a film having magnesium fluoride as a main component, not more than 5 wt.% oxygen, and not more than 1.5 wt.% magnesium **oxide**; or a **film** having magnesium fluoride as a main component, and 1-10 wt.% rare gas.

ADVANTAGE - The formed fluorine-containing thin film has a high transmittance for ultraviolet light, particularly, vacuum ultraviolet light; is capable of effectively using the light; and is less damaged by negative ions, positive ions, and electrons.

DESCRIPTION OF DRAWING(S) - The figure is a schematic view of a sputtering apparatus used in the invented process.

Vessel 10
Target 13
Discharge space 18
Sputtering gas 30
Fluorine-containing gas 31
Anode 41
Substrate 70
DC power 80
Dwg.1A/14

L4 ANSWER 11 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2001-280725 [29] WPIX
DNN N2001-200124 DNC C2001-085166
TI Formation of narrow deep trench isolation on semiconductor substrate by forming, patterning, and etching pad and barrier layers to form first trench, forming buffer oxide spacers, etching bottom of first trench to form second trench.
DC L03 U11
IN CHEN, S; LIN, C J; SHIH, J
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6207532 B1 20010327 (200129)* 10p
ADT US 6207532 B1 US 1999-408494 19990930
PRAI US 1999-408494 19990930
AB US 6207532 B UPAB: 20010528

NOVELTY - A narrow deep trench isolation on semiconductor substrate is formed by forming, patterning, and etching pad and barrier layers to form first trench; forming buffer oxide spacers; etching bottom of first trench to form second trench; removing buffer oxide spacers; depositing and polishing second **oxide layer**; and performing N neg.
and P neg. well implants and performing N pos. and P pos. implants.

DETAILED DESCRIPTION - Formation of narrow deep trench isolation on semiconductor substrate consists of (a) forming a pad layer on surface of substrate and a barrier layer on pad layer; (b) patterning the barrier and the pad layers to form an opening; (c) etching the substrate through the opening to form a first trench having sloping sidewalls and bottom; (d) growing first **oxide layer** on surfaces of patterned
barrier and pad **layers**; (e) forming buffer **oxide**
spacers on sidewalls of first trench; (f) etching the substrate on the bottom of first trench to form a second trench having sloping sidewalls; (g) removing buffer oxide spacers; (h) depositing second **oxide**
**layer** on surface of patterned barrier layer; (i) chemical
mechanical polishing the second **oxide layer**; (j)
performing N neg. and P neg. well implants on surface of the substrate;

and (k) performing N pos. and P pos. implants around the periphery of first trench. The cross-section surface area of first and second trenches in a plane that is parallel with the surface of the substrate decreases in size, respectively. The N neg. and P neg. well implants are aligned with, adjacent to, and on opposite sides of first and second trenches.

USE - For forming narrow deep trench isolation on semiconductor substrate.

ADVANTAGE - The method creates deep trench without increasing trench angle.

Dwg.0/10

L4 ANSWER 12 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2001-272690 [28] WPIX
DNN N2001-194707 DNC C2001-082636
TI Manufacture of semiconductor device, e.g. metal-oxide semiconductor transistor, by using salicide process for removing residue on substrate surfaces.
DC L03 U11
IN BESSER, P R; CHAN, S S; HUI, A T; NGO, M V
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 1
PI US 6204136 B1 20010320 (200128)* 8p
ADT US 6204136 B1 US 1999-386466 19990831
PRAI US 1999-386466 19990831
AB US 6204136 B UPAB: 20010522

NOVELTY - A semiconductor device is made by using salicide process where residue on substrate surfaces resulting from reactive plasma etching for sidewall spacer formation is removed prior to salicide processing.

DETAILED DESCRIPTION - Manufacture of a semiconductor device by providing a semiconductor substrate having a surface. A thin gate **insulator layer** (5) is formed in contact with the substrate surface. A gate electrode is formed on a portion of the gate **insulator layer**. The gate electrode comprises two opposing side surfaces and a top surface. A blanket **layer** of an **insulative** material is formed on the exposed portions of the thin gate **insulator layer** on the substrate surface and on the two opposing side surfaces and top surface of the gate electrode. The blanket **layer** of **insulative** material and underlying portions of the thin gate **insulator layer** from the substrate surface, and the blanket **layer** of **insulative** material from the top surface of the gate electrode are removed by anisotropically etching, thus forming an insulative sidewall spacer (9') on each opposing side surface of the gate electrode and each exposing portion of the substrate surface adjacent the sidewall spacers. The residue and/or contaminants resulting from anisotropically etching of the exposed portions of substrate surface are removed.

USE - For manufacturing semiconductor devices, e.g. metal-oxide semiconductor (MOS) or complementary MOS transistors.

ADVANTAGE - The invention enables formation of reliable, defect-free, low junction leakage, sub-micron-dimensioned MOS transistors and CMOS devices at rates consistent with the requirements at manufacturing throughput, and is fully compatible with conventional process flow for automated manufacture of high-density integration semiconductor devices.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional schematic view of a MOS transistor.

Thin gate **insulator layer** 5
Insulative sidewall spacer 9'
Electrically conductive silicide 11, 12, 12'

Dwg.3/3

L4 ANSWER 13 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2001-101706 [11] WPIX
DNN N2001-075467 DNC C2001-029605
TI Formation of a sharp poly tip in split-gate flash cell for use as a semiconductor device comprises etching a nitride layer through a photoresist mask with pattern corresponding to the floating gate of the cell.
DC L03 U11 U12 U13 U14
IN HSIEH, C; KUO, D; LIN, Y; SUNG, H; YEH, J
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6165845 A 20001226 (200111)* 11p
ADT US 6165845 A US 1999-298931 19990426
PRAI US 1999-298931 19990426
AB US 6165845 A UPAB: 20010224
NOVELTY - A sharp poly tip (147) in a split-gate flash memory cell is formed by etching a nitride layer through a photoresist mask with pattern corresponding to the floating gate of the cell to form an opening with tapered profile, growing gate **oxide** (120) **layer** at opening's bottom, and forming a first polysilicon layer (160) and an interpoly **oxide layer** (170) over a substrate (100).

DETAILED DESCRIPTION - Formation of a sharp poly tip in a split-gate flash memory cell comprises subsequently forming a pad **oxide layer** and a nitride layer over silicon substrate, patterning a photoresist layer to form a mask corresponding to a floating gate of the cell, etching the nitride layer to form an opening with tapered profile, subsequently removing the photoresist **layer** and the pad **oxide layer**, growing gate **oxide layer** at a bottom of the opening, forming a first polysilicon layer over the substrate, performing chemical-mechanical polishing and oxidizing the first polysilicon layer, subsequently removing the first photoresist **layer** and the pad **oxide layer** exposed at the opening's bottom, forming an interpoly **oxide layer** over the substrate, forming and patterning a second polysilicon layer with the photoresist mask having control gate (180) pattern to complete the formation of flash memory cell with sharp poly tip.

USE - For forming poly tip in split-gate flash cell e.g., flash electrically erasable programmable read only memories (EEPROMs) cell, for use as a semiconductor device.

ADVANTAGE - The method is simpler and provides sharper and more robust poly tip with improved erase speed in split-gate flask memory and less susceptible to damage during the manufacture of the cell.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a semiconductor substrate portion.

Substrate 100
Gate oxide 120
Poly tip 147
First polysilicon layer 160
Interpoly **oxide layer** 170
Control gate 180
Dwg.3i/3

L4 ANSWER 14 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2001-079598 [09] WPIX
DNN N2001-060561 DNC C2001-022807
TI Manufacture of a split-gate flash memory cell involves etching back an isolation oxide in a trench to form a three-dimensional coupling source region.

DC L03 U11 U12 U13 U14
IN HSIEH, C; KUO, D; LIN, Y; SUNG, H; YEH, J
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6159801 A 20001212 (200109)* 20p
ADT US 6159801 A US 1999-298932 19990426
PRAI US 1999-298932 19990426
AB US 6159801 A UPAB: 20010213
NOVELTY - A split-gate flash memory cell is manufactured by forming an isolation trench, lining the trench with a conformal oxide, and etching back an isolation oxide in the trench to form a three-dimensional coupling source region in the upper portion of the trench to allow three-dimensional flow of electrons from the coupling region into a floating gate of the cell.

DETAILED DESCRIPTION - Formation of a split-gate flash memory cell comprises:

(a) forming a pad **oxide layer** over a substrate (100), a first nitride layer, patterning a first photoresist layer to define active regions in the substrate, and a trench by etching;

(b) removing the first photoresist layer;

(c) forming a conformal lining on the inside walls of the trench;

(d) depositing isolation oxide to form a shallow trench isolation (STI);

(e) performing chemical-mechanical polishing;

(f) removing the first nitride and pad **oxide layers**;

(g) forming and patterning a second photoresist layer to define three-dimensional coupling region in the trench;

(h) etching back the oxide in the trench to form a three-dimensional coupling source region (405) in the upper portion of the trench to allow flow of electrodes from the coupling region to a floating gate (380) of the cell;

(i) removing the second photoresist layer;

(j) forming and removing sacrificial **oxide layer**;

(k) growing gate **oxide layer** (375) and sidewalls of the three-dimensional coupling region in the trench;

(l) forming first polysilicon layer to fill the coupling region in the upper portion of the trench, a second nitride layer, and patterning a third photoresist layer to define a cell area and floating gate;

(m) etching the pattern in the third photoresist to expose the first polysilicon layer and then removing the third photoresist;

(n) oxidizing the exposed first polysilicon **layer** to form poly-**oxide** (385) using the second nitride as a mask;

(o) removing the second nitride layer and then etching the first polysilicon layer to form floating gate using the poly-oxide as hard mask;

(p) forming inter-poly oxide and a second polysilicon layer (420);

(q) forming and patterning a fourth photoresist layer to form a control gate region, etching the pattern then removing the fourth photoresist;

(r) forming and patterning a fifth photoresist layer to define source implant region, performing source implantation and then removing the fifth photoresist layer;

(s) forming spacers on the side-walls of the control gate; and

(t) forming drains of the split-gate flash memory cell.

USE - The method is used for forming a split-gate flash memory cell having the three-dimensional source capable of three-dimensional coupling with the floating gate of the cell.

ADVANTAGE - The method provides a split-gate flash memory having the three-dimensional source to increased lateral coupling ratio between the

source and the floating gate. The sidewall of the floating gate which forms the third dimension provides the extra area through which the coupling ratio is increased. The higher coupling ratio is achieved without an increase in the cell size and at the same time alleviating the punchthrough and junction break-down of the source region by sharing gate voltage along the side-wall.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of the substrate showing the formation of three-dimensional region of the trench.

Substrate 100

Source region 405

Gate **oxide layer** 375

Floating gate 380

Poly-oxide 385

Second polysilicon layer 420

Dwg.5G/5

L4 ANSWER 15 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2001-049161 [06] WPIX
DNN N2001-037636 DNC C2001-013459
TI Formation of a stacked-gate flash memory by depositing a high nitride **layer** over the pad **oxide layer**, forming a shallow trench isolation filled with isolation oxide, and forming a self-aligned source regions.
DC L03 U11 U13 U14
IN CHEN, J; HSIEH, C; KUO, D; LIN, C J; LIN, Y; SU, H
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6153494 A 20001128 (200106)* 13p
ADT US 6153494 A US 1999-310257 19990512
PRAI US 1999-310257 19990512
AB US 6153494 A UPAB: 20010126

NOVELTY - A stacked-gate flash memory is formed by depositing a high or thick nitride **layer** over the pad **oxide layer**, forming a shallow trench isolation (STI) filled with isolation **oxide** through the nitride **layer** into the substrate; and forming a self-aligned source regions in the substrate.

DETAILED DESCRIPTION - Formation of a stacked-gate flash memory having shallow trench isolation with a high-step oxide and high lateral coupling includes forming a pad **oxide layer** (210) over a semiconductor substrate (100). A high nitride layer (220) is formed over the pad **oxide layer**. A first photoresist layer is formed and patterned over the high nitride layer to define active regions in the substrate. A trench (230) is formed in the substrate, by etching through patterns in the first photoresist layer, which is then removed. A conformal lining is formed on the inside walls of the trench. An isolation oxide (250) is deposited inside the trench to form shallow trench isolation (STI) with a high-step oxide. A chemical mechanical polishing (CMP) of the substrate is performed. The nitride layer is removed to form high steps. The pad **oxide layer** is removed at the bottom of the high steps. A sacrificial **oxide layer** is then formed over the substrate. The sacrificial **oxide layer** is then removed. A floating gate **oxide layer** is grown over the substrate. A first polysilicon layer is formed conformally over the high steps. A second photoresist layer is formed and patterned over the substrate to define the first polysilicon layer and form floating gate regions in the substrate. The first polysilicon layer is etched to form floating gates. A second photoresist layer is removed. An interpoly oxide is formed over the floating gates. A

second polysilicon layer is formed over the interpoly **oxide layer**. A third photoresist layer is formed and patterned over the interpoly **oxide layer** to define control gate and word line. It is then etched through patterning to form the word line. A fourth photoresist layer is formed and patterned over the substrate to define self-aligned source (SAS) regions in the substrate. The SAS regions are etched, followed by the removal of the fourth photoresist layer.

USE - For forming a stacked-gate flash memory for use in semiconductor devices.

ADVANTAGE - The method provides a step-up in the shallow trench isolation in a stacked-gate flash memory cell without any increase in the lateral dimensions of the cell.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the substrate with STI formed through a thick nitride layer.

Substrate 100

Pad **oxide layer** 210

Nitride layer 220

Trench 230

Isolation oxide 250

Dwg.3b/3

L4 ANSWER 16 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2001-017079 [03] WPIX
DNN N2001-012909 DNC C2001-004897
TI Etching **oxide layer** on nitride **layer**, comprises preparing plasma derived from carbonaceous and fluorine-containing gas and gas containing nitrogen, and etching in plasma.
DC L03 U11
IN BENNETT, D A; NORUM, J P; YAN, H; YU, C
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 5
PI DE 10016938 A1 20001116 (200103)* 5p
JP 2001023957 A 20010126 (200110) 6p
US 6294102 B1 20010925 (200158)
KR 2001020758 A 20010315 (200159)
SG 83790 A1 20011016 (200176)
ADT DE 10016938 A1 DE 2000-10016938 20000405; JP 2001023957 A JP 2000-131682 20000428; US 6294102 B1 US 1999-305432 19990505; KR 2001020758 A KR 2000-20550 20000419; SG 83790 A1 SG 2000-2138 20000413
PRAI US 1999-305432 19990505
AB DE 10016938 A UPAB: 20010116
NOVELTY - Process for etching an **oxide layer** located on a nitride layer in the upper region of a substrate having a high etching selectivity for the **oxide layer** comprises preparing a plasma derived from a carbonaceous and fluorine-containing gas and a gas containing nitrogen, and etching the substrate in the plasma.

USE - In the production of semiconductors.

ADVANTAGE - The substrate has high selectivity for the **oxide layer**.

Dwg.0/1

L4 ANSWER 17 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2000-664317 [64] WPIX
CR 1997-288767 [26]; 1998-495064 [42]; 2000-022285 [02]; 2002-236893 [06]
DNN N2000-492274 DNC C2000-201223
TI Fabrication of a capacitor in an integrated circuit involves forming a contact via through a silicon nitride **layer** and depositing a **dielectric** material into the contact via.

DC L03 U11 U12 U13 U14
IN NEW, D C
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6133108 A 20001017 (200064)* 9p
ADT US 6133108 A CIP of US 1995-559186 19951113, Div ex US 1996-650915 19960517, US 1998-113743 19980710
FDT US 6133108 A CIP of US 5631804, Div ex US 5801916
PRAI US 1996-650915 19960517; US 1995-559186 19951113; US 1998-113743 19980710
AB US 6133108 A UPAB: 20020508
NOVELTY - A capacitor is fabricated in an integrated circuit by forming a silicon nitride layer in direct contact with the bottom electrode. A contact via is formed on the silicon nitride **layer**. A **dielectric** material having a dielectric constant of greater than 100 is deposited into the contact via, and a top electrode is formed on the dielectric material.

DETAILED DESCRIPTION - Fabrication of a capacitor in an integrated circuit involves forming a bottom electrode (20) in electrical contact with a circuit node of the integrated circuit. A silicon nitride layer (26) is formed in direct contact with the bottom electrode. A contact via (30) is formed through the silicon nitride layer to partially expose the bottom electrode. A dielectric material (40) having a dielectric constant of greater than 100 is deposited into the contact via, and a top electrode is formed on the dielectric material.

USE - For fabricating a capacitor in an integrated circuit.

ADVANTAGE - The method fabricates a capacitor having a high dielectric constant and of uniform thickness. It avoids chemical or physical breakdown of the dielectric material, or short-circuiting across the capacitor electrodes.

DESCRIPTION OF DRAWING(S) - The figure illustrates the method of fabricating the capacitor in an integrated circuit.

Bottom electrode 20
Silicon nitride layer 26
Contact via 30
Dielectric material 40
Overflow portion(50) Top conductive layer 42

Dwg.6/7

L4 ANSWER 18 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2000-610692 [58] WPIX
DNN N2000-452202 DNC C2000-182550
TI Enclosing copper conductors in protective barrier in manufacture of integrated circuit chips, involves forming copper layer over barrier on hole trench structure and covering copper with another barrier.
DC G06 L03 P84 U11
IN JANG, S
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6110648 A 20000829 (200058)* 10p
ADT US 6110648 A US 1998-156058 19980917
PRAI US 1998-156058 19980917
AB US 6110648 A UPAB: 20001114
NOVELTY - A composite hole trench structure is formed using lower and upper level **dielectric layers** (120a,120b) by successive etching. The structure is covered by a barrier layer (160). Copper deposit (170) is provided over the structure which is etched back to have cavities after planarizing. The deposit is covered by another barrier layer (165) which is removed partially, enclosing the copper

layer.

DETAILED DESCRIPTION - An oxide or low-k polymer lower level **dielectric** (LLD) **layer** (120a) of thickness 5000-8000 Angstrom is formed on a substrate (100) which has devices on it and a metal layer. An etch stop layer is formed on the LLD layer over which an upper level **dielectric** (ULD) **layer** (120b) of same composition and thickness 500-9000 Angstrom is formed. A photoresist of thickness 1.2 mu m is formed over the ULD layer and is patterned to have a hole pattern using a photomask. The hole pattern is formed up to etch stop layer by etching. The photoresist layer is removed by oxygen plasma ashing and another photoresist layer is formed which is patterned to have a trench pattern using a photomask. Conductive line trenches are etched on the ULD layer till the etch stop layer using the photoresist. The hole pattern in the ULD layer is transferred to LLD layer till the lower level of the substructure of the substrate by further etching so that a composite hole and trench structure is formed. The photoresist layer is removed by oxygen plasma ashing. A barrier layer (160) of thickness 150-300 Angstrom is formed by depositing titanium nitride covering all the parts. A copper deposit (170) is formed over the composite hole and trench structure covering the barrier layer. The metal layer is planarized by chemical mechanical polishing (CMP) and subjected to partial etch back to form cavities over the metal layer. The whole structure is covered with another barrier layer (165) of titanium nitride composition and thickness 500-1000 Angstrom . The portions of the barrier layer are removed by CMP, leaving the portions over the cavity to encase the metal layer between the barrier layers. During the removal of the barrier layer by CMP the table speed is set as 20-60 rpm, the pad pressure is set as 28-70 kPa and slurry flow rate is 100-200 standard cubic centimeters per minute (sccm). Alternately a trench pattern is formed first and the hole pattern is formed next while forming the composite hole trench structure.

USE - For enclosing copper wiring interconnects over semiconductor substrate in damascene process in manufacture of ultra large scale integrated (ULSI), very large scale integrated (VLSI) circuit chips.

ADVANTAGE - Forms copper dual damascene interconnect encased in barrier to protect surrounding insulation material from diffusion of copper.

DESCRIPTION OF DRAWING(S) - The figure shows the formation of copper interconnect.

Substrate 100

Lower level **dielectric layer** 120a

Upper level **dielectric layer** 120b

Barrier layer 160

Barrier layer 165

Copper deposit 170

Dwg.3F/4

L4 ANSWER 19 OF 55 WPIX (C) 2002 THOMSON DERWENT

AN 2000-490314 [43] WPIX

DNN N2000-363843 DNC C2000-147238

TI Formation of a sharp poly tip to improve erase speed in a split-gate flash memory cell includes etching process using a top-oxide as a hard mask to form floating gate.

DC L03 U11

IN HSIEH, C; KUO, D; LIN, C; LIN, Y; SUNG, H; YEH, J

PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO

CYC 1

PI US 6090668 A 20000718 (200043)* 11p

ADT US 6090668 A US 1999-248725 19990211

PRAI US 1999-248725 19990211

AB US 6090668 A UPAB: 20000907
NOVELTY - A sharp poly tip is formed by providing a first polysilicon **layer** on the gate **oxide layer**. A high pressure etch is performed to form a recess with a sloped profile in the first polysilicon **layer**. A top-**oxide layer** is deposited on the recess. Etching is performed using the top-oxide as a hard mask to form floating gate.

DETAILED DESCRIPTION - Formation of a sharp poly tip to improve erase speed in a split-gate flash memory cell comprises providing a silicon substrate (100) having active and field regions defined. A gate **oxide layer** (130) is formed on the substrate. A first polysilicon layer (140) is formed on the gate **oxide layer**. A nitride **layer** (150) is formed on the first polysilicon layer. A first photoresist layer (160) is formed and patterned to form a photoresist mask (165) with a pattern corresponding to the floating gate of the split-gate flash memory cell. The nitride layer is etched through the photoresist mask to form openings (155) and to expose portions of the first polysilicon layer. A high pressure etch is performed to form a recess (143) with a sloped profile (141) in the first polysilicon layer. The first photoresist layer is removed. A top-**oxide layer** is deposited on the recess and overfills the recess extending into the opening in the nitride **layer**. The top-**oxide layer** is partially removed from the opening in the nitride layer. The nitride layer is removed. Etching is performed using the top-oxide as a hard mask to etch portions of the first polysilicon layer not covered by the top-oxide to form floating gate. An interpoly oxide is formed on the top-**oxide layer**. A second polysilicon layer is deposited on the interpoly **oxide**. The second polysilicon **layer** is patterned with a second photoresist mask having control gate pattern to form a control gate.

USE - For forming a sharp poly tip to improve erase speed in a split-gate flash memory cell used in flash electrically erasable programmable read only memories (EEPROMs).

ADVANTAGE - The invention reduces the variation of memory erasing speed resulting from the non-uniformity of the bird's beak in split-gate flash cells. It forms a poly tip without poly oxidation.

DESCRIPTION OF DRAWING(S) - The figures show cross-sectional views of the semiconductor substrate.

Silicon substrate(130) Gate **oxide layer** 100
First polysilicon layer 140
Sloped profile(143) Recess 141
nitride layer 150
Openings 155
First photoresist layer 160
Photoresist mask 165
3b, 3c/3

L4 ANSWER 20 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2000-482032 [42] WPIX
DNN N2000-358315 DNC C2000-144997
TI Formation of borderless contact used in ultra large scale integrated circuit chip manufacture involves using a metal contact plug etch-back process.
DC L03 U11
IN HO, C; SUN, Y; TSAI, C
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6083824 A 20000704 (200042)* 10p
ADT US 6083824 A US 1998-114132 19980713

PRAI US 1998-114132 19980713
AB US 6083824 A UPAB: 20000905
NOVELTY - A borderless contact is formed using a metal contact plug etch-back process.

DETAILED DESCRIPTION - Formation of borderless contact comprises providing a semiconductor substrate (110) having a substructure comprising device and/or metal **layers**; forming an interlevel **dielectric** (ILD) and/or intermetal **dielectric** (IMD) **layer** (200) over the substrate; planarizing the ILD/IMD layer; forming a first photoresist layer over the hard-mask layer; patterning the first photoresist layer with a line trench pattern; etching through the line trench pattern in the first photoresist layer to form a line trench opening in the hard-mask layer (300); removing the first photoresist layer; forming a second photoresist layer over the hard-mask layer having line trench opening; patterning the second photoresist layer with a hole contact pattern; etching through the contact hole pattern in the second photoresist layer to form a contact hole opening in the ILD/IMD layer until the substructure is reached; removing the second photoresist layer; forming a glue layer (600) on the wall of the contact hole opening; depositing a plug metal (700) in the contact hole opening; performing etch-back of the plug metal half way down the depth of the contact hole opening; etching further the line trench opening in the hard-mask layer into half way down the thickness of the ILD/IMD layer; forming metal over the substrate having the line trench opening; and removing the metal from the surface of the substrate for subsequent process steps to complete the fabrication of a semiconductor substrate.

USE - The method is used for forming a borderless contact or interconnects in a semiconductor substrate. The method is used in manufacture of ultra large scale integrated (ULSI) circuit chips.

ADVANTAGE - The invention eliminates one photoresist mask, has self alignment capability, and easy photoresist stripping and cleaning. It also increases the over-all manufacturability of borderless interconnects.

DESCRIPTION OF DRAWING(S) - The figure shows an interconnect comprising a borderless contact or via hole.

Substrate 110
**Dielectric layer** 200
Hard-mask layer 300
Glue layer 600
Plug metal 700
Dwg.3i/3

L4 ANSWER 21 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2000-475739 [41] WPIX
DNN N2000-354916 DNC C2000-142608
TI Plasma etching of **oxide layer** using etching gas containing **fluorocarbon**, nitrogen, oxygen, inert gas and hydrogen containing gas.
DC L03 U11
IN HILLS, G; KEIL, D; KHAJEHNOURI, K; NGUYEN, T D; NGUYEN, T
PA (LAMR-N) LAM RES CORP
CYC 24
PI WO 2000039846 A1 20000706 (200041)* EN 26p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: IL JP KR SG
US 6217786 B1 20010417 (200123)
EP 1147549 A1 20011024 (200171) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
ADT WO 2000039846 A1 WO 1999-US31077 19991228; US 6217786 B1 US 1998-223963 19981231; EP 1147549 A1 EP 1999-968192 19991228, WO 1999-US31077 19991228

FDT EP 1147549 A1 Based on WO 200039846
PRAI US 1998-223963 19981231
AB WO 200039846 A UPAB: 20000831
NOVELTY - Plasma etching of **oxide layer** (704) involves flowing etching gas comprising **fluorocarbon**, nitrogen reactant gas, oxygen reactant gas, inert carrier gas and hydrogen containing additive. Plasma is formed from the etching gas.
USE - Plasma etching of **oxide layer** for fabrication of integrated circuit.
ADVANTAGE - The etching gas is very selective to the photoresist (706).
DESCRIPTION OF DRAWING(S) - The figure shows a cross section of the layer stack with deep and narrow opening and vertical walls.
Silicon **oxide layer** 704
Photoresist 706
Dwg.7/7

L4 ANSWER 22 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2000-472616 [41] WPIX
DNN N2001-000012 DNC C2001-000003
TI Fabrication of a short-wavelength optoelectronic device useful as e.g. recording medium involves injection of a highly energetic electron beam to create electron hole-pairs, recombination of which produce oscillating photons.
DC A32 A89 L03 U11 U12
IN BAEK, M C; CHO, G I; CHOI, S W; LEE, H G; SHIM, G H; CHO, K I; SHIM, K H
PA (KOEL-N) KOREA ELECTRONICS & TELECOM RES INST; (ELTE-N) ELECTRONICS & TELECOM RES INST
CYC 2
PI KR 99051077 A 19990705 (200041)*
US 6139760 A 20001031 (200101)B 9p
KR 279737 B 20010201 (200210)
ADT KR 99051077 A KR 1997-70316 19971219; US 6139760 A US 1998-129880 19980806; KR 279737 B KR 1997-70316 19971219
FDT KR 279737 B Previous Publ. KR 99051077
PRAI KR 1997-70316 19971219
AB US 6139760 A UPAB: 20001230 ABEQ treated as Basic
NOVELTY - Fabrication of a short-wavelength optoelectronic device formed from a wide band gap material by a cathodoluminescence involves injection of a highly energetic electron beam to create electron-hole pairs, and oscillating photons are produced by the electron-hole recombination.
DETAILED DESCRIPTION - Fabrication of the optoelectronic device including a junction of an optical device and a field emission device array which emits ultraviolet wavelength and short-wavelength waves comprises: a) sequentially depositing a superlattice buffer layer, a wave guide layer, a quantum well layer, and a Bragg diffraction superlattice layer on an optoelectronic device substrate (1); b) depositing a first **insulating layer** (2), a first metal **layer** (3), a second **insulating layer** (4) and a second metal layer (5) in a laminated form, forming a mask pattern on (5) and etching the layers from the exposed (5) to (1) and forming a via hole exposing the surface of the superlattice buffer layer formed on (1); c) forming a light reflection layer on the bottom surface of the via hole; d) etching the Bragg diffraction layer, the quantum well layer and the wave guide layer on (1) to have a mesa structure and depositing a cathode metal layer on the mesa structure to prepare the optical device; e) depositing (2), (3), (4), (5), a high voltage **insulating layer** and a third metal layer in a laminated form on a field emission device substrate; f) etching (2), (3), (4), (5), third metal layer and a high voltage

**insulating layer** from the uppermost laminate by use of a photoresist pattern to form an opening exposing the surface of the field emission device substrate and forming a grid metal, a first acceleration electrode and a first focusing electrode on (1); g) forming a cathode tip on the exposed substrate to prepare a field emission device array (6); and h) adhesively combining the optical device and (6) being separated at a predetermined distance from each other by support pillars.

USE - As optical recording medium for displays, medical appliances and measuring instruments.

ADVANTAGE - The short-wavelength laser enhances the optical record density several giga bytes such that the capacity of data communication device such as multimedia information server can be greatly increased. The laser eliminates the need of using dopants for forming n - p junctions in the semiconductor and achieving high efficiency in terms of energy because highly energetic electrons result in one or more electron-hole pair.

Dwg.0/3

AB KR 99051077 A UPAB: 20010110

NOVELTY - Fabrication of a short-wavelength optoelectronic device formed from a wide band gap material by a cathodoluminescence involves injection of a highly energetic electron beam to create electron-hole pairs, and oscillating photons are produced by the electron-hole recombination.

DETAILED DESCRIPTION - Fabrication of the optoelectronic device including a junction of an optical device and a field emission device array which emits ultraviolet wavelength and short-wavelength waves comprises: a) sequentially depositing a superlattice buffer layer, a wave guide layer, a quantum well layer, and a Bragg diffraction superlattice layer on an optoelectronic device substrate (1); b) depositing a first **insulating layer** (2), a first metal **layer** (3), a second **insulating layer** (4) and a second metal layer (5) in a laminated form, forming a mask pattern on (5) and etching the layers from the exposed (5) to (1) and forming a via hole exposing the surface of the superlattice buffer layer formed on (1); c) forming a light reflection layer on the bottom surface of the via hole; d) etching the Bragg diffraction layer, the quantum well layer and the wave guide layer on (1) to have a mesa structure and depositing a cathode metal layer on the mesa structure to prepare the optical device; e) depositing (2), (3), (4), (5), a high voltage **insulating layer** and a third metal layer in a laminated form on a field emission device substrate; f) etching (2), (3), (4), (5), third metal layer and a high voltage **insulating layer** from the uppermost laminate by use of a photoresist pattern to form an opening exposing the surface of the field emission device substrate and forming a grid metal, a first acceleration electrode and a first focusing electrode on (1); g) forming a cathode tip on the exposed substrate to prepare a field emission device array (6); and h) adhesively combining the optical device and (6) being separated at a predetermined distance from each other by support pillars.

USE - As optical recording medium for displays, medical appliances and measuring instruments.

ADVANTAGE - The short-wavelength laser enhances the optical record density several giga bytes such that the capacity of data communication device such as multimedia information server can be greatly increased. The laser eliminates the need of using dopants for forming n - p junctions in the semiconductor and achieving high efficiency in terms of energy because highly energetic electrons result in one or more electron-hole pair.

Dwg.0/3

L4 ANSWER 23 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2000-375522 [32] WPIX
DNN N2000-282045 DNC C2000-113363

TI Dual damascene structure formation, using highly selective oxynitride etching stop layer to prevent cracking.

DC L03 P61 U11
IN CHAO, L; FU, C; LIAW, J; TSAI, C
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6063711 A 20000516 (200032)* 9p
ADT US 6063711 A US 1998-69456 19980428
PRAI US 1998-69456 19980428
AB US 6063711 A UPAB: 20000706

NOVELTY - Formation of dual damascene structure involves utilizing a highly selective etching stop layer (650) of oxynitride. The layer is formed over an intermetal **dielectric** (IMD) **layer** (600) formed over a semiconductor substrate (100).

DETAILED DESCRIPTION - The formation of dual damascene structure comprises:

(a) providing a semiconductor substrate having a substructure comprising devices formed in the substrate and a metal layer;

(b) forming a first (IMD) layer over the substrate;

(c) forming a high-selectivity etch stop layer over the first IMD layer;

(d) forming a second IMD layer over the etch-stop layer;

(e) forming a first photoresist layer over the second IMD layer and patterning the photoresist layer with a mask comprising a line trench pattern;

(f) etching through the line trench pattern in the first photoresist layer until the etch-stop layer is reached to form the line trench into the second IMD layer;

(g) removing the first photoresist layer;

(h) forming a second photoresist layer over the second IMD layer including the line in the second IMD layer;

(i) patterning the second photoresist layer with a mask comprising a via hole pattern;

(j) etching through the via hole pattern in the second photoresist layer into the etch-stop layer, thus forming a via hole opening in the etch-stop layer;

(k) etching further through the via hole opening in the etch-stop layer to form the via hole pattern into the first IMD layer;

(l) removing the second photoresist layer;

(m) depositing metal in the line trench and the via hole composite structure; and

(n) removing the metal from the surface of the substrate for subsequent process steps to complete the fabrication of a semiconductor substrate.

The forming of the high-selectivity etch-stop layer is accomplished by reacting SiH4 with N2O and **NH3** at 300-40 deg. C by CVD to form oxynitride having a thickness of 500-1,500 Angstrom . The etching of the via hole is accomplished with a recipe comprising gases such as **CF4** with a flow rate of 80-90 sccm, CHF3 at 10-20 sccm, and Ar at 180-200 sccm.

USE - For forming damascene structures useful in the manufacture of semiconductor substrates.

ADVANTAGE - Provides a high selectivity etching stop layer with a specific chemistry and smaller thickness, thus preventing cracking during damascene process as well as the associated problems of poor definition of contact or via holes in the damascene structure.

DESCRIPTION OF DRAWING(S) - The figure shows the formation of the first IMD layer and the oxynitride etch-stop layer.

Semiconductor substrate 100

IMD layer 600
Etching stop layer 650
Dwg.3a/3

L4 ANSWER 24 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2000-338333 [29] WPIX
DNN N2000-253950 DNC C2000-102612
TI Forming copper damascene interconnects using chemical-mechanical polishing of the etch-stop layer by first lining the inside walls with a diffusion barrier layer and depositing a copper metal into the dual damascene structure.
DC L03 U11
IN JANG, S
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6051496 A 20000418 (200029)* 10p
ADT US 6051496 A US 1998-156052 19980917
PRAI US 1998-156052 19980917
AB US 6051496 A UPAB: 20000617
NOVELTY - Copper damascene interconnects are formed using chemical-mechanical polishing of the etch-stop layer by first lining the inside walls of a dual damascene structure with a diffusion barrier layer; and depositing a copper metal into the damascene structure.
DETAILED DESCRIPTION - A method of using an etch-stop layer for chemical-mechanical polishing (CMP) of copper (190) damascene comprises a) providing a semiconductor substrate having a substructure comprising devices formed in the substrate and a metal layer being formed; b) forming a dual damascene structure having a groove (180) and a hole over the substructure; c) forming a barrier layer (115) covering the substrate including the inside walls of the damascene structure; d) forming metal in the damascene structure; e) forming an etch-stop layer (200) over the substrate covering the metal; f) performing a first CMP of the substrate to remove the etch-stop layer from higher regions and expose underlying the metal forming exposed regions while leaving the etch-stop layer as a protective layer over lower regions (210) on the substrate; g) etching the metal in the exposed regions (220'); and h) performing a second CMP for global planarization of the substrate.
USE - For forming copper damascene interconnects using chemical-mechanical polishing of the etch-stop layer.
ADVANTAGE - The invention provides damascene copper interconnects with reduced CMP dishing.
DESCRIPTION OF DRAWING(S) - The figure shows the partial CMP of the etch-stop layer from high regions of the underlying copper metal.
LLD layer 110
Barrier layer 115
Groove 180
Copper 190
Etch-stop layer 200
Lower regions 210
Exposed regions 220'
Dwg.3b/3

L4 ANSWER 25 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2000-316765 [27] WPIX
CR 2002-163103 [03]
DNN N2000-237759 DNC C2000-095700
TI Formation of split-gate flash memories by forming gate oxide with appropriate thicknesses between the substrate, the floating gate and the control gate along with an extra thin nitride layer formed over the

primary gate **oxide layer**.

DC L03 U11 U12 U13 U14
IN HSIEH, C; KUO, D; LIN, Y; SUNG, H; YEH, C
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6046086 A 20000404 (200027)* 8p
ADT US 6046086 A US 1998-100691 19980619
PRAI US 1998-100691 19980619
AB US 6046086 A UPAB: 20020403
NOVELTY - Split-gate flash memories are formed with correct gate oxide (120, 150) thicknesses between the substrate (100), the floating gate and the control gate (190) along with an extra thin nitride layer (130) formed over the primary gate **oxide layer**.

DETAILED DESCRIPTION - Split-gate flash memories with improved data retention capacity and increased coupling ratio are formed by providing a silicon substrate with defined active and field areas; forming a gate **oxide layer** over the substrate; depositing a nitride **layer** over the gate **oxide layer**; forming a photoresist layer over the nitride layer; patterning the photoresist layer to define a cell area and a source size; etching to pattern the nitride **layer** and the gate **oxide layer** corresponding to the cell area; removing the photoresist layer from the substrate; forming a second gate **oxide layer** adjacent to the patterned **oxide** and nitride **layers**; forming a polysilicon layer over the substrate; forming a second nitride layer over the polysilicon layer; forming a second photoresist layer over the second nitride layer; patterning the second photoresist layer to define a floating gate region on the substrate; etching the second nitride layer through second photoresist and forming openings reaching the polysilicon layer; performing ion implantation through the openings of the second patterned photoresist layer to form source/drain regions (111, 113) within the substrate; removing the second photoresist layer; performing thermal oxidation of the polysilicon layer exposed in the openings to form regions of poly-oxide (135); removing the second nitride layer; etching the polysilicon layer using the regions of the poly-oxide as a mask; growing inter-poly oxide (180) over the polysilicon layer; forming a second polysilicon layer over the inter-poly oxide; and patterning the second polysilicon layer to form a control gate and complete the forming of the memory cell.

USE - For forming split-gate flash memory.

ADVANTAGE - The split-gate flash memory cell has increased capacitive coupling, improved programmability and has reduced size.

DESCRIPTION OF DRAWING(S) - The figure shows the completion of the split-gate flash memory cell with the forming of the inter-poly oxide and the control gate.

Substrate 100
Source 111
Drain 113
Gate oxide 120
Nitride layer 130
Poly-oxide caps 135
Second gate **oxide layer** 150
Inter-poly oxide 180
Control gate 190
Dwg.3i/3

L4 ANSWER 26 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 2000-022317 [02] WPIX
DNN N2000-016548 DNC C2000-005376

TI Silicon oxide deposition.
DC L03 U11
IN IYER, R; SANDHU, G S
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 5985770 A 19991116 (200002)* 3p
ADT US 5985770 A US 1997-915987 19970821
PRAI US 1997-915987 19970821
AB US 5985770 A UPAB: 20020213
NOVELTY - Silicon oxide deposition comprises: (a) combining a silicon gas with hydrogen peroxide at -10 to 30 deg. C to deposit liquid silicon oxide precursor on substrate; (b) gas phase doping the precursor using dopants provided as plasma proximate the deposited liquid precursor; (c) increasing temperature of deposited precursor and polymerising the precursor; and (d) raising the temperature of the polymerised precursor and forming a solid doped silicon **oxide**-containing **layer** on the substrate.
USE - Used for deposition of silicon oxide(s) on a substrate is semiconductor device manufacture.
Dwg.0/0

L4 ANSWER 27 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 1999-478075 [40] WPIX
DNN N1999-355839 DNC C1999-140600
TI Forming trenches in a substrate, with controlled etch bias for semiconductor device manufacture.
DC A89 G06 L03 U11
IN NGUYEN, P L; SCHWEINFURTH, R A; SIVAKUMAR, S
PA (ITLC) INTEL CORP
CYC 1
PI US 5933759 A 19990803 (199940)* 12p
ADT US 5933759 A US 1996-778020 19961231
PRAI US 1996-778020 19961231
AB US 5933759 A UPAB: 19991004
NOVELTY - Trenches are formed in a substrate for semiconductor device manufacture by performing three etch steps through a polish stop or hard mask **layer**, an underlying **oxide layer** and a silicon substrate.
DETAILED DESCRIPTION - Trenches are formed in a substrate by: performing a first etch with a first carbon-fluorine etchant through a polish stop layer or hard mask **layer** and an **oxide layer**, the first etch forming polymer on exposed surfaces; performing a second etch with a second carbon-fluorine etchant to remove the polymer; and performing a third etch, preferably with a non carbon-fluorine etchant, through the substrate. Preferably the substrate is silicon or polysilicon and the polish stop or hard mask layer is silicon nitride. The trench is etched through a photoresist pattern mask.
USE - In manufacture of semiconductor devices.
ADVANTAGE - The process provides improved etch selectivity and etch bias so that smaller and more dense devices may be fabricated. Trenches are formed with submicron critical dimensions, aspect ratios above 2:1, photoresist selectivity above 15:1 and an etch bias within 0.05 micron.
Dwg.0/4

L4 ANSWER 28 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 1999-357858 [30] WPIX
DNN N1999-266401 DNC C1999-105934
TI Forming diamond-like carbon coatings onto particles of e.g., powdered dyes and pigments, semiconductors etc..

DC A35 L03 M13 M22 P53 U11
IN DAVID, M M
PA (MINN) MINNESOTA MINING & MFG CO; (MINN) 3M INNOVATIVE PROPERTIES CO
CYC 84
PI WO 9927157 A1 19990603 (199930)* EN 33p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
AU 9896878 A 19990615 (199944)
US 6015597 A 20000118 (200011)
EP 1034320 A1 20000913 (200046) EN
R: DE FR GB IT
US 6197120 B1 20010306 (200115)
TW 414726 A 20001211 (200124)
CN 1279729 A 20010110 (200128)
KR 2001032454 A 20010425 (200164)
JP 2001524603 W 20011204 (200203) 40p
EP 1034320 B1 20011219 (200206) EN
R: DE FR GB IT
DE 69803096 E 20020131 (200216)
ADT WO 9927157 A1 WO 1998-US21111 19981007; AU 9896878 A AU 1998-96878 19981007; US 6015597 A US 1997-979072 19971126; EP 1034320 A1 EP 1998-950973 19981007, WO 1998-US21111 19981007; US 6197120 B1 Div ex US 1997-979072 19971126, US 1999-382169 19990824; TW 414726 A TW 1998-118313 19981104; CN 1279729 A CN 1998-811433 19981007; KR 2001032454 A KR 2000-705695 20000525; JP 2001524603 W WO 1998-US21111 19981007, JP 2000-522295 19981007; EP 1034320 B1 EP 1998-950973 19981007, WO 1998-US21111 19981007; DE 69803096 E DE 1998-603096 19981007, EP 1998-950973 19981007, WO 1998-US21111 19981007
FDT AU 9896878 A Based on WO 9927157; EP 1034320 A1 Based on WO 9927157; US 6197120 B1 Div ex US 6015597; JP 2001524603 W Based on WO 9927157; EP 1034320 B1 Based on WO 9927157; DE 69803096 E Based on EP 1034320, Based on WO 9927157
PRAI US 1997-979072 19971126; US 1999-382169 19990824
AB WO 9927157 A UPAB: 19990802
NOVELTY - The particles are agitated in a chamber supplied with a carbon source and having capacitatively coupled electrodes, one grounded and one to which radio frequency (RF) power is supplied so that a reactive plasma is generated adjacent to the particles and an ion sheath continually surrounds them.

USE - Formation of densely packed diamond-like transparent coatings on **oxide-coated** phosphor particles. Also formation of carbon-hydrogen-silicon coatings on silicon carbide abrasive particles and coatings on polyethylene beads, powdered dyes and pigments, semiconductors, metal compounds, and metal-coated particles. Applications include magnetic rigid disks, sunglasses, ophthalmic lenses and windows.

ADVANTAGE - Efficient deposition of dense coatings at high deposition rates. Surface cleaning of particles can be carried out in situ. Bulk and surface properties of coatings can be varied by adjustment of operating parameters. Deposition temperature is lower than for diamond coatings.
Dwg.0/2

L4 ANSWER 29 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 1998-387042 [33] WPIX
DNN N1998-301826 DNC C1998-117012
TI Reduction of surface contamination in post chemical mechanical polishing

(CMP) cleaning - by CMP and a scrubbing and subsequent plasma treatment to remove first and second thickness of surface.

DC L03 U11
IN CHANG, C; JANG, S; YU, C
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 1
PI US 5773360 A 19980630 (199833)* 6p
ADT US 5773360 A US 1996-734067 19961018
PRAI US 1996-734067 19961018
AB US 5773360 A UPAB: 19980819
A CMP process for polishing a plasma enhanced tetraethylorthosilicate (PETEOS) or borophosphoro TEOS layer by using a slurry and etchant to remove a first thickness (5000 - 15000 deg. A) of an upper silicon **oxide layer**, scrubbing the polished layer to remove particulate contamination preferably in the presence of **ammonia** solution, and then a dry plasma etch to remove a second thickness (50 - 500 deg. A). The slurry is alumina in KOH or NH4OH solution. The dry etch is a parallel plate etcher or downstream plasma etcher using **CF4** or CHF3.

USE - Chemical mechanical polishing of substrates.

ADVANTAGE - The process results in reduced particulate contamination and the surface is microscopically smooth and free of residual mobile ions.

Dwg.0/5

L4 ANSWER 30 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 1998-035216 [04] WPIX
CR 1997-538384 [50]
DNN N1998-028283 DNC C1998-011949
TI Etching **dielectric layers** at high etch rates, high selectivity ratios etc. - using plasma formed from mixture of fluoro-hydrocarbon, **ammonia**-generating, oxy carbon and optionally **fluorocarbon** and inert gases.
DC L03 U11
IN DING, J C; SHAN, H; WELCH, M; DING, J
PA (MATE-N) APPLIED MATERIALS INC
CYC 20
PI EP 813233 A2 19971217 (199804)* EN 16p
R: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
JP 10056001 A 19980224 (199818) 12p
US 5814563 A 19980929 (199846)
ADT EP 813233 A2 EP 1997-304035 19970610; JP 10056001 A JP 1997-147995 19970605; US 5814563 A CIP of US 1996-639388 19960429, US 1996-660966 19960612
PRAI US 1996-660966 19960612; US 1996-639388 19960429
AB EP 813233 A UPAB: 19981118
A method of etching a **dielectric layer** supported by a silicon wafer or other substrate comprises: (a) placing the substrate supporting the **dielectric layer** in a process zone; (b) etching the **dielectric layer** using a plasma formed from a process gas comprising (i) fluoro-hydrocarbon gas for forming fluorine-containing etchant species; (ii) **ammonia**-generating gas having a liquefaction temperature LT of -60 to 20 deg. C; and (iii) oxycarbon gas; and (c) the substrate and **dielectric layer** are maintained at (LT-50) deg. C to (LT+50) deg. C.

USE - In addition to silicon oxide, the process can be used to etch, e.g. silicides, borides, nitrides, and carbides. The process is useful in semiconductor integrated circuit fabrication to electrically isolate devices or features formed on the substrate (e.g. monocrystalline silicon,

polysilicon layers, anti-reflective or diffusion barrier layers, e.g. titanium silicide or titanium nitride); or for etching holes between interconnect lines, the holes being subsequently filled with electrically conductive material to form vertical interconnects (holes or vias) to connect devices formed on the substrate or to interconnect lower levels of interconnect lines to upper levels of interconnect lines.

ADVANTAGE - High etching selectivity ratios of etching silicon oxide to polysilicon, e.g. > 100:1, etching profile angles higher than 85 deg. , and silicon oxide etch rates of 600-900 nm/minute (9000 Angstrom /minute), providing large processing windows under a range of different process conditions.

Dwg.0/7

L4 ANSWER 31 OF 55 WPIX (C) 2002 THOMSON DERWENT

AN 1996-141238 [15] WPIX

DNN N1996-118247 DNC C1996-044492

TI Semiconductor device with improved operating speed - has interlayer **insulating layers** of amorphous carbon film.

DC L03 U11

IN ENDO, K

PA (NIDE) NEC CORP; (NIDE) NIPPON ELECTRIC CO

CYC 8

PI EP 701283 A2 19960313 (199615)* EN 38p
R: DE FR GB NL
JP 08083842 A 19960326 (199622) 5p
CA 2157257 A 19960313 (199626)
JP 08222557 A 19960830 (199645) 7p
JP 08236517 A 19960913 (199647) 8p
JP 08264648 A 19961011 (199651) 5p
EP 701283 A3 19961113 (199701)
US 5698901 A 19971216 (199805) 34p
JP 2751851 B2 19980518 (199825) 6p
JP 10116908 A 19980506 (199828) 6p
JP 10261716 A 19980929 (199849) 6p
CA 2157257 C 19990810 (199952) EN
US 6033979 A 20000307 (200019)
KR 188573 B1 19990601 (200055)

ADT EP 701283 A2 EP 1995-114253 19950911; JP 08083842 A JP 1994-217470 19940912; CA 2157257 A CA 1995-2157257 19950830; JP 08222557 A JP 1995-21429 19950209; JP 08236517 A JP 1995-35023 19950223; JP 08264648 A JP 1995-64066 19950323; EP 701283 A3 EP 1995-114253 19950911; US 5698901 A US 1995-526902 19950912; JP 2751851 B2 JP 1995-21429 19950209; JP 10116908 A Div ex JP 1994-217470 19940912, JP 1997-296721 19940912; JP 10261716 A Div ex JP 1995-64066 19950323, JP 1998-59511 19950323; CA 2157257 C CA 1995-2157257 19950830; US 6033979 A Div ex US 1995-526902 19950912, US 1997-782573 19970110; KR 188573 B1 KR 1995-29566 19950911

FDT JP 2751851 B2 Previous Publ. JP 08222557

PRAI JP 1995-64066 19950323; JP 1994-217470 19940912; JP 1995-21429 19950209; JP 1995-35023 19950223; JP 1997-296721 19940912; JP 1998-59511 19950323

AB EP 701283 A UPAB: 19960417

A semiconductor device has interlayer **insulating layers** composed of an amorphous carbon film.

Also claimed are (a) a method of fabricating the semiconductor device with an F-contg. amorphous C **film** as interlayer **insulating film** by PECVD of a mixt. of (i) at least one of **CF4**, **C2F6**, **C3F8**, **C4F8** and CHF3 and (ii) at least one of N2, NO, NO2, **NH3** and NF3, (b) a method as in (a) using a mixt. of (i) as above and (ii) at least one of SiH4,

SiH6 and SiF4, and (c) a method of fabricating the device with an F-contg. amorphous C **insulating film** by PECVD using CxFy gas where x = 1-4 and y = 4-8.

USE - For MOSFETs.

ADVANTAGE - The interlayer **insulating layers** have low **dielectric** constant and thus reduce wire delay, allowing the device to operate at higher speed. The C film has higher heat resistance than polyimide, and no humidity occurs in the film during polymerisation. Dwg.3/25

L4 ANSWER 32 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 1995-217279 [29] WPIX
DNN N1995-170241 DNC C1995-100489
TI Plasma etching silica selectively w.r.t. silicon nitride and poly silicon - using **ammonia**- nitrogen tri fluoride mixt. as plasma gas and converting oxide to ammonium hexa fluorosilicate.
DC L03 U11
IN BARNES, M S; CHAPPLE-SOKOL, J D; COTLER, T J; HOLBER, W M; KELLER, J H; PODLESNIK, D
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 4
PI EP 658928 A1 19950621 (199529)* EN 12p
R: DE FR GB
US 5505816 A 19960409 (199620) 11p
ADT EP 658928 A1 EP 1994-480102 19941007; US 5505816 A US 1993-168887 19931216
PRAI US 1993-168887 19931216
AB EP 658928 A UPAB: 19950727
A method of selectively etching an **oxide layer** comprises generating a plasma of reactive radicals in a chamber (16) contg. a substrate (18) having an **oxide layer** and exposing for sufficient time to permit a desired portion of the **oxide** to form prod. **layers** contg. ammonium hexafluorosilicate.

Also claimed is a non-selective method of etching oxides as above which consumes the **oxides** to prod. **layers** at equal rates.

Also claimed is a method as above in which the plasma gas mixt. (14) comprises **NH3**/NF3 or **CF4**/)2 mixed in H2 and N2. and the **oxide layer** is initially formed on the substrate independently of the etching step.

USE - For selectively etching **oxide films** on Si wafers, both natural and other **oxide films**, and in etching vias and trenches.

ADVANTAGE - Wet HF processing is avoided, there is no polymer formation, and different types of oxide are etched non-selectively. Dwg.1/5

L4 ANSWER 33 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 1994-083442 [10] WPIX
CR 1993-258449 [32]
DNN N1994-065162 DNC C1994-038266
TI Increased dielectric strength in capacitors - by exposure of metal foil, dielectric and/or the fully assembled capacitor to lower pressure, low temp. gas plasma.
DC A35 A85 L03 P42 V01
IN BINDER, M; LAVENE, B; MAMMONE, R J
PA (USSA) US SEC OF ARMY; (USGO) US GOVERNMENT
CYC 25
PI WO 9405024 A1 19940303 (199410)* EN 23p

RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: AU BR CA FI JP KP KR RU
US 5305178 A 19940419 (199415) 8p
AU 9334415 A 19940315 (199428)
ADT WO 9405024 A1 WO 1993-US209 19930113; US 5305178 A CIP of US 1991-743660 19910812, CIP of US 1992-829194 19920203, US 1992-931618 19920818; AU 9334415 A AU 1993-34415 19930113
FDT AU 9334415 A Based on WO 9405024
PRAI US 1992-931618 19920818
AB WO 9405024 A UPAB: 19940608
A capacitor with increased dielectric breakdown strength is produced by (a) providing a non-conductive dielectric; (b) providing a metal foil; (c) exposing at least one of the above to a gas plasma; and (d) placing the dielectric and the metal foil together to form a capacitor.

Also claimed are (i) a method as above in which the non-conductive dielectric is formed from a resin; (ii) a method in which at least part of a capacitor is exposed to a gas plasma; and (iii) a capacitor produced by the above methods.

The gas plasma is pref. from O2, He, N2, **NH3**, CO2, **CF4**/O2 or water vapour, esp. a mixt. of 96% **CF4** and 4% O2. Exposure is pref. from 0.5-8 min., pref. at 300-500 mTorr and 10-60 deg.C. The dielectric may be a thermoplastic-based film; from polycarbonate, polypropylene, polyvinylidene fluoride or polyester; or at least one of a polymer, a copolymer or a ceramic.

USE - In the prodn. of capacitors for use in the storage or delivery of large amts. of electrical current, e.g. in power plants, hand-held portable equipment, high-efficiency, high-energy power supplies, pacemakers, filtering applications, etc.
Dwg.1/2

L4 ANSWER 34 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 1990-180497 [24] WPIX
CR 1990-161412 [21]
DNN N1990-140276 DNC C1990-078313
TI Carbon based film deposited on silicon nitride coated glass substrate - obtd. by deposition from plasma decomposed gases such as silane and **ammonia** for the nitride and ethylene for the carbon.
DC L02 L03 M13 P42 P73 U11
IN HAYASHI, S; ISHIDA, N; ITOU, K; KADONO, M; KOJIMAK, M; SASAKI, M; TAKEYAMA, J; YAMAZAKI, S; KOJIMA, M
PA (SEME) SEMICONDUCTOR ENERGY LAB
CYC 7
PI EP 372696 A 19900613 (199024)* 6p
R: DE FR GB
JP 02259058 A 19901019 (199048)
CN 1041790 A 19900502 (199106)
US 5185179 A 19930209 (199308) 10p
EP 372696 B1 19950104 (199506) EN 15p
R: DE FR GB
DE 68920417 E 19950216 (199512)
KR 9411007 B1 19941122 (199642)
JP 3025808 B2 20000327 (200020) 4p
ADT EP 372696 A EP 1989-310429 19891010; JP 02259058 A JP 1989-82015 19890331; US 5185179 A US 1989-417311 19891005; EP 372696 B1 EP 1989-310429 19891010; DE 68920417 E DE 1989-620417 19891010, EP 1989-310429 19891010; KR 9411007 B1 KR 1989-14465 19891010; JP 3025808 B2 JP 1989-82015 19890331
FDT DE 68920417 E Based on EP 372696; JP 3025808 B2 Previous Publ. JP 02259058
PRAI JP 1988-255491 19881011; JP 1989-82015 19890331
AB EP 372696 A UPAB: 20000426

Substrates such as glass which are to be coated with a carbonaceous film are first coated wtih a nitride (e.g. silicon nitride) film to prevent penetration of carbon into the substrate.

The nitride is deposited by applying high frequency alternating voltages, thereby creating a plasma state, to a gas contg. e.g. silane and **ammonia**. The carbonaceous film is deposited in a similar way from a gas contg. a hydrocarbon. A fluorine cpd. such as a **carbon fluoride** may also be present of fluorine makes the carbonaceous film hydrophilic. Pref. the carbonaceous film is composed of diamond-like carbon.

Part only of the substrate may selectively coated by protecting part of the substrate with a mask and scratching the part no so covered. A diamond film is grown on the scratched surface through chemical vapour reaction. The scratching step may be done by dipping the substrate in a fluid in which diamond powder is dispersed and subjecting to ultrasonic vibration.

USE - Forming abrasion-proof films on vehicle window glass. @(6pp Dwg.No.7b/7)@

7b/7

L4 ANSWER 35 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 1987-261415 [37] WPIX
DNN N1987-195536 DNC C1987-110934
TI Monocrystalline thin film mfr. - by selective removing **oxide film** on polycrystalline material and recrystallising.
DC L03 U11
PA (MATE) MATSUSHITA ELECTRONICS CORP
CYC 1
PI JP 62182186 A 19870810 (198737)* 3p
ADT JP 62182186 A JP 1986-21442 19860203
PRAI JP 1986-21442 19860203
AB JP 62182186 A UPAB: 19930922
Method comprises forming an **oxide film** over the surface of a polycrystalline film to be monocrystallised, removing the **oxide film** partially, and recrystallising the polycrystalline film by melting.

ADVANTAGE - Explosion of the **oxide film** and the polycrystalline film which may occur upon the melting of the polycrystalline film is avoided.

In an example (1) is Si base plate; (2) is SiO2 film (ca. 0.9 micron); (3) is poly-Si LOCOS **oxide film**; (4) is poly-Si film (0.5 micron); (5) is SiO2 film (50 micron); (6) is nitride film (0.12 micron). By heating the base plate 1 for four hours in a steam environment at 1000 deg.C the surface is oxidised. The poly-Si film (4) is deposited by pyrolysis of SiH4 gas at 600 deg.C under reduced pressure. The nitride layer (6) is then deposited by the reaction of **NH3** and SiH2Cl2 at 750 deg.C in reduced-pressure CVD, and patterning is effected by photolithography using **CF4** and O2 as the etchants in the plasma etching. Then LOCOS growth is carried out in water vapour at 1020 deg.C for six hours and remaining nitride film is removed with hot concentrated phosphoric acid. Finally the SiO2 film (5) is formed by heating in dry oxygen at 1000 deg.C for 30 mins.

1,2,3/3

L4 ANSWER 36 OF 55 WPIX (C) 2002 THOMSON DERWENT
AN 1986-116144 [18] WPIX
DNN N1986-085357 DNC C1986-049558
TI Plasma CVD treatment device - in which silicon-hydride and **ammonia** in nitrogen carrier gas are introduced into vacuum vessel contg. aluminium

electrodes.
DC L03 M14 U11
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 61056415 A 19860322 (198618)* 3p
JP 06069032 B2 19940831 (199433) 3p
ADT JP 61056415 A JP 1984-153414 19840724; JP 06069032 B2 JP 1984-153414 19840724
FDT JP 06069032 B2 Based on JP 61056415
PRAI JP 1984-153414 19840724
AB JP 61056415 A UPAB: 19930922
In device using plasma for formation of **insulating layer** on semiconductor element (e.g. IC, LSI, etc) SiH4 and **NH3** are introduced, together with N2 or Ar gas as carrier gas, into reactor container kept under vacuum condition and discharge is made between upper and lower aluminium electrodes in such a way as to grow Si3N4 on surface of wafer (e.g. of Si) heated to 300-400 deg.C. Conductor constitutes high frequency current path and holds discharge electrode in device made of stainless steel base material coated with aluminium.
USE/ADVANTAGE - Device has highly corrosion resistant conductor part and enables dry etching for plasma CVD treatment using **CF4** gas to be performed readily and also reduces number of cleaning processes.
1,2/2

L4 ANSWER 37 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 2000-331992 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN MIYATA KOJI
PA SONY CORP
PI JP 2000331992 A 20001130 Heisei
AI JP1999-138302 (JP11138302 Heisei) 19990519
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To provide an etching method by which a material film containing organic elements can be etched anisotropically without alteration and no **carbon fluoride** gas is required in consideration of the environmental problem such as global warming.
SOLUTION: This manufacturing method is used to etch a material **film** (a first **insulation film** 12 and a second **insulation film** 15) which contains at least silicon, carbon, oxygen, and halogen element and satisfies an equation, 2A+2B<2C+D (assuming that the element ratio of silicon, carbon, oxygen, and halogen element is Si:C:O:Halogen element = A:B:C:D) by using a gas plasma containing at least one kind or a plurality of kinds among carbon monoxide, hydrogen, nitrogen, **ammonia**, water, and rare gas. The material film is etched by dissolving it by a plasma for gasification.
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L4 ANSWER 38 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1997-260350 JAPIO
TI PLASMA ETCHING METHOD OF **OXIDE** SILICON-BASED **INSULATING FILM**
IN YANAGIDA TOSHIHARU
PA SONY CORP, JP (CO 000218)
PI JP 09260350 A 19971003 Heisei
AI JP1996-62417 (JP08062417 Heisei) 19960319
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 10
AB PURPOSE: TO BE SOLVED:To obtain excellent selection ratio to substratum material layers and a resist mask, and reduce microloading effect and

particle contamination, by using mixture gas which contains gas containg N and H as constituent elements and gas containing C and F as constituent elements.
CONSTITUTION: licon **oxide**-based **insulating film** 3 on substratum material layers 1, 2 is patterned by using mixture gas which contains gas containing N and H as constituent elements and gas containing C and F as constituent elements. For example, the silicon **oxide**-based **insulating film** 3 composed of SiO2 is formed on a semiconductor substrate 1 of Si or the like on which an impurity diffusion layer 2 or the like is previously formed. A resist mask 4 having an aperture diameter of 0.25.mu.m is patterned on a connection hole aperture position. Then an exposed part of the silicon **oxide**-based **insulating film** 3 is plasma etched with mixture gas of **C3F8** and **NH3** by using a magnetron RIE equipment which jointly uses an magnetic field, and a contact hole 5 is formed.

L4 ANSWER 39 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1993-206126 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN AOKI HIDEMITSU
PA NEC CORP, JP (CO 000423)
PI JP 05206126 A 19930813 Heisei
AI JP1992-38487 (JP04038487 Heisei) 19920129
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1464, Vol. 17, No. 636, P. 149 (19931125)
AB PURPOSE: To obtain an etching method accompanied by no generation of an after-corrosion, by performing through an **NH3** gas and a CH3OH gas a dry- etching for processing a Cu film finely.
CONSTITUTION: When a Cu film 3 is processed finely by a dry-etching and a semiconductor device is manufactured, the dry-etching is performed using an **NH3** gas and a CH3OH gas. For example, a foundational **oxide film** 2 is formed on an Si substrate 1, and thereon, a Cu film 3 is formed by a sputtering or CVD method. Then, on the Cu **film** 3, an **oxide film** 4 by the CVD method is formed, and by applying a photoresist film 5 thereto, the patterning of the **oxide film** 4 is performed. Subsequently, the **oxide film** 4 laid on the Cu film 3 is patterned by the dry-etching using **CF4** and CHF3 gases, and it is used as a mask material when processing the Cu film 3. Then, after removing the resist 5 left on the **oxide film** 4 by an 02 gas plasma, using the **oxide film** 4 for masking as a mask, the dry-etching of the Cu film 3 is performed by a mixed gas of an **NH3** gas and a CH3OH gas.

L4 ANSWER 40 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1992-186844 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN MARUO YUTAKA
PA SEIKO EPSON CORP, JP (CO 000236)
PI JP 04186844 A 19920703 Heisei
AI JP1990-317554 (JP02317554 Heisei) 19901121
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1281, Vol. 16, No. 5, P. 77 (19921019)
AB PURPOSE: To prevent short-circuiting and current leak between a gate and a source and between a gate and a drain, by etching high melting point metal on a side wall by dry etching, and thinly etching the side wall surface by dry etching.
CONSTITUTION: The following processes are contained. Polycrystalline

silicon 104 is deposited on a gate **insulating film** 103 formed on an element formation region on a semiconductor substrate. Said polycrystalline silicon 104 is etched in the manner in which a region turning to the gate electrode of a MOS transistor is left. A side wall 107 is formed on the edge part of said polycrystalline silicon 104. High melting point metal is sputtered on the whole surface of the substrate. The high melting point metal is made to react with Si by heat treatment. The high melting point metal on the side wall 107 is etched by wet etching. The side wall surface is thinly etched by dry etching. For example, wet etching is performed by using aqueous **ammonia**, and then dry etching is performed by using mixed gas of CHF3 and **CF4**

L4 ANSWER 41 OF 55 JAPIO COPYRIGHT 2002 JPO

AN 1992-158552 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN MOROZUMI YUKIO
PA SEIKO EPSON CORP, JP (CO 000236)
PI JP 04158552 A 19920601 Heisei
AI JP1990-284054 (JP02284054 Heisei) 19901022
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1266, Vol. 16, No. 447, P. 151 (19920917)
AB PURPOSE: To improve humidity resistance and an effect of contamination resistance and to improve the reliability of a miniaturized semiconductor device by a method wherein a first silicon nitride film is formed, a spacer is formed on the side wall of a metal wiring by anisotropic etch back and then a second silicon nitride film is formed on the occasion when a protective **insulation film** is formed.
CONSTITUTION: After metal wirings 14 and 15 are formed, a first silicon nitride film 16 is made to grow by bringing SiH4 and **NH3** into a plasma reaction with N2, used as a carrier. Next, anisotropic etch back is applied by **CF4**, C2, F6 and 02, so that a spacer constituted of the silicon nitride film 16 is formed in the side wall parts of the metal wirings, and then a sintering process is executed. Next, a second silicon nitride film 17 is deposited by a plasma reaction and then subjected to sective dry etching, and thereby a bonding pad 19 for extraction of an external electrode is opened.

L4 ANSWER 42 OF 55 JAPIO COPYRIGHT 2002 JPO

AN 1991-167828 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN MOROZUMI YUKIO
PA SEIKO EPSON CORP, JP (CO 000236)
PI JP 03167828 A 19910719 Heisei
AI JP1989-308210 (JP01308210 Heisei) 19891128
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1123, Vol. 15, No. 4, P. 76 (19911017)
AB PURPOSE: To improve reliability of a protecting film by carrying out vapor growth of SiO2 on a final metal wiring of a semiconductor device, by treating it at a temperature higher than its formation temperature, by providing a spacer on a sidewall through anisotropic etching and by covering it with Si2N4 through SiO2 and plasma reaction.
CONSTITUTION: After an Al wiring 14 whose side surface is vertical is formed on an Si substrate 11, an SiO2 film is deposited through vapor reaction of organic silane at a growth temperature of 370 to 380.degree.C. Then, after treatment at 450.degree.C in Ar of 3% H2, **C2F6**+CHF3 is used for anisotropic etch back to make an SiO2 spacer 15 remain. It is covered with a PSG film 16 and an Si3N4 film 17 is overlaid thereon through plasma reaction in SiH4+**NH3**+N2 using a parallel plate. A

resist mask is used to shape an electrode window 18 by etching. According to this constitution, it is possible to improve distortion balance and evenness of a protecting **insulating film**, to improve humidity resistance, anti-migration characteristics, etc., thereof and to improve reliability.

L4 ANSWER 43 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1991-155640 JAPIO
TI MANUFACTURE OF MOS TYPE SEMICONDUCTOR DEVICE
IN MOROZUMI YUKIO
PA SEIKO EPSON CORP, JP (CO 000236)
PI JP 03155640 A 19910703 Heisei
AI JP1989-295519 (JP01295519 Heisei) 19891114
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1118, Vol. 15, No. 39, P. 1 (19911003)
AB PURPOSE: To improve yield, electrical characteristics and reliability by forming the sidewall spacer of the gate electrode, etc., of a MOS transistor in the laminated structure of a silicon nitride **film** and a silicon **oxide film** and preventing the over-etching of a field **oxide film** and a gate **oxide film** when the spacer is shaped.
CONSTITUTION: A silicon nitride film 27 is grown in a gas atmosphere containing SiH4 and **NH3**, and a silicon **oxide film** 17 acquired by vapor-phase reacting SiH4 and O2 at approximately 400.degree.C is laminated. A spacer 18 is formed on the sidewall of a gate electrode 14 through anisotropic etch-back by a reactive dry etcher containing **C2F6** and CHF3 gas. The emission spectrum 337nm of N from the foundation silicon nitride film 27 is received and desired over-etch is conducted for the time of the reception in the detection of an end point at the time of the anisotropic etch-back of the silicon **oxide film** 17 at that time, but etch-back is performed positively because the silicon nitride film 27 is shaped onto the whole foundation surface while a selection ratio is taken to the silicon nitride film 27, thus preventing the etching of a field **oxide film** 12 and a gate **oxide film** 13 on a source and a drain.

L4 ANSWER 44 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1991-148122 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN KATAMI KAZUHIKO
PA SEIKO EPSON CORP, JP (CO 000236)
PI JP 03148122 A 19910624 Heisei
AI JP1989-286504 (JP01286504 Heisei) 19891102
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1113, Vol. 15, No. 371, P. 149 (19910918)
AB PURPOSE: To prevent corrosion by depositing a polymer film containing carbon, hydrogen, fluorine on the surface of a wafer, removing the film dipped in an organic solvent, then dipping it in an alkaline solution, neutralizing and removing chlorine and chloride that remain on the surface of a semiconductor substrate.
CONSTITUTION: Methane trifluoride is introduced as reaction gas into a vacuum vessel, a high frequency is applied to be discharged to decompose and polymerize it to form a **carbon fluoride** polymer film 107 containing carbon, hydrogen, fluorine as ingredients on the sidewall of titanium nitride 103, aluminum-copper alloy 104 and the surface of a silicon **oxide film** 102 and aluminum-copper alloy 104. Then, it is dipped in acetone, the film 107 is dissolved, removed, and then continuously dipped in dilute **ammonia**

water. Here, chloride 106 that remains on the sidewall of the nitride 103, the alloy 104 and the surface of the film 102 and the alloy 104 is completely neutralized and removed. Thus, corrosion can be prevented.

L4 ANSWER 45 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1989-175257 JAPIO
TI MANUFACTURE OF MIS SEMICONDUCTOR DEVICE
IN SAITO TSUTOMU; NAKAMURA MORITAKA; SATO YASUHISA
PA FUJITSU LTD, JP (CO 000522)
PI JP 01175257 A 19890711 Heisei
AI JP1987-332228 (JP62332228 Heisei) 19871229
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 831, Vol. 13, No. 453, P. 13 (19891011)
AB PURPOSE: To prevent a tungsten gate electrode from being side-etched and to prevent an irregularity and a deterioration of the performance of an element by a method wherein, after a gate **insulating film** and a tungsten layer have been formed on a semiconductor substrate and this assembly has been thermally nitrified in **ammonia** gas, a patterning operation is executed by reactive ion etching using a fluorine-based gas.
CONSTITUTION: A gate **oxide film** 5 by thermal oxidation is formed in a device formation region 4 on a p- type Si substrate 1; then, a W layer 106 is formed by a sputtering method. Then, this assembly is heat-treated in **ammonia** gas; a tungsten nitride layer 7 is formed. Then, an SiO2 mask film 108 is formed; a resist pattern 9 corresponding to a gate electrode is formed on it; an SiO2 mask pattern 8 corresponding to the gate electrode is formed by making use of the resist pattern as a mask by an RIE operation using a gas of CHF3+**CF4**; in addition, the W layer 106 is patterned by making use of the mask pattern as a mask by the RIE operation using a gas ot SF6. By this setup, the side- etching amount e1 on the side of a W gate electrode 6 can be reduced to about 500-1000.ANG. or less.

L4 ANSWER 46 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1989-133323 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN TAKEDA YOSHIYA
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 01133323 A 19890525 Heisei
AI JP1987-292357 (JP62292357 Heisei) 19871119
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 811, Vol. 13, No. 383, P. 57 (19890824)
AB PURPOSE: To perform microetching of a layer without giving no damage to a foundation by using gas for etching containing the first gas having fluorine as a constituent and the second gas having nitrogen as a constituent so as to etch the **layer** formed on tantalum **oxide**.
CONSTITUTION: Fluorine hydrocarbon system gas such as **CF4**, CHF3, nitrogen fluoride such as NF3 and XeF are used as the first gas containing fluorine as a constituent, while nitrogen oxide such as N2, N2O and **NH3**, NF3 are used as the second gas. A means, which generally excites a substance, such as plasma discharge, ultraviolet ray radiation may do as a means for forming the first and the second gas mentioned above into radicals and ions of fluorine and nitrogen. A radical of fluorine reacts on Si to become silicon fluoride and tantalum becomes gas called tantalum fluoride having high vapor pressure so as to advance etching. Here, under existing fluorine, the radical of nitrogen is excluded from advancing to silicon nitride by reacting on Si. However, in the case of tantalum, reaction on tantalum nitride having low vapor pressure on the

tantalum surface advances even under existing fluorine to prevent further etching so as to obtain a large etching selection ratio.

L4 ANSWER 47 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1989-093173 JAPIO
TI MANUFACTURE OF GAAS FIELD EFFECT TRANSISTOR
IN TAMURA AKIYOSHI
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 01093173 A 19890412 Heisei
AI JP1987-251028 (JP62251028 Heisei) 19871005
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 792, Vol. 13, No. 325, P. 162 (19890721)
AB PURPOSE: To improve on Schottky barrier .vphi.B and gm by a method wherein a very thin GaN layer is formed between an N-type GaAs active layer and a gate electrode.
CONSTITUTION: A photoresist film 2 serves as a mask in a process of implanting Si29 ions 101 into a GaAs substrate 1 for the formation of an N-type active layer 3. The entirety is processed in an **NH3** gas plasma for the conversion of the surface of the GaAs substrate 1 into a GaN thin film 4. Next, the entire surface is covered by a WSi film 5 that is formed by spattering, which is followed by etching in a **CF4** /O2 gas for the formation of a gate electrode 6. After formation of an SiO2 side wall 7, Si28 ions 100 are implanted for the formation of an N+ region 8. An SiO2 **insulating film** 9 is formed to cover the entire surface, and then an AuGe/Au source electrode 10 and drain electrode 11 are constructed for the completion of a FET of this design. A Schottky barrier .vphi.B as well as gm may be enhanced in the presence of a very thin GaN layer, which produces a high performance FET.

L4 ANSWER 48 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1988-236357 JAPIO
TI SEMICONDUCTOR DEVICE
IN OZEKI NOBORU
PA NEC CORP, JP (CO 000423)
PI JP 63236357 A 19881003 Showa
AI JP1987-71288 (JP62071288 Showa) 19870324
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 709, Vol. 13, No. 38, P. 89 (19890127)
AB PURPOSE: To prevent the resistivity of a poly Si layer from increasing and to eliminate the dispersion of the characteristics of a semiconductor device by a method wherein a resistor, which is used for the device and consists of the poly Si film, or the upper and lower **insulating films** of the lead-out electrode part of a transistor are constituted of an Si nitride film.
CONSTITUTION: Silane gas, **ammonia** gas and so on are thermally decomposed on an Si substrate 1 at about 650.degree.C to form by vapor growth an Si nitride film 2 of a thickness of 1000-3000 .ANG. as a lower **insulating film** and thereafter, a resistor 3 consisting of a 2000-4000 .ANG. thick poly Si film, wherein boron of 1.times.414-5.times.1014 piece/cm3, for example, is ion-implanted, is formed. Then, the resistor 3 is coated with a 1000-2000 .ANG. thick Si nitride film 4 as an upper **insulating film**. After that, resistance electrode lead-out opening parts are provided in the film 4 by plasma etching using **CF4** and so on and a semiconductor device, wherein Al electrodes 5 consisting of an Al layer of 0.5-1.0 .mu.m or thereabouts are formed and which is connected with other terminals, is constituted.

L4 ANSWER 49 OF 55 JAPIO COPYRIGHT 2002 JPO

AN 1987-159437 JAPIO
TI SEMICONDUCTOR ELEMENT
IN TSUDA SHIGERU
PA FUJI ELECTRIC CO LTD, JP (CO 000523)
PI JP 62159437 A 19870715 Showa
AI JP1986-1020 (JP61001020 Showa) 19860107
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 568, Vol. 11, No. 396, P. 128 (19871224)
AB PURPOSE: To prevent a nitride film of an upper layer from overhanging by forming the nitride film of a 2-layer protecting **film** of an **oxide film** and the nitride film on a silicon substrate of a nitride having 2.05 or lower of refractive index.
CONSTITUTION: An **oxide film** 3 is formed on a silicon substrate 1 having a P-N junction 2, and the film 3 is covered with a nitride film 6 having lower refractive index than that of a conventional nitride film. Such a nitride film is generated by enhancing the mixture ratio of **NH3** of reaction gas to SiH4 in case of plasma CVD. A resist film 5 is patterned on the film 6, and plasma etched with mixture gas of **CF4** and O2. Then, when the film 3 is etched with fluoric acid etchant, the film 6 thereon is simultaneously etched to eliminate overhangs. The etching property of the nitride film is obtained when the refractive index of the film 6 is 2.06 or lower.

L4 ANSWER 50 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1984-076444 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN SHIOZAKI MASAKAZU
PA TOSHIBA CORP, JP (CO 000307)
PI JP 59076444 A 19840501 Showa
AI JP1982-187850 (JP57187850 Showa) 19821026
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 262, Vol. 8, No. 1851, P. 125 (19840824)
AB PURPOSE: To prevent generation of bird beak by forming Si3N4 at the side surface of triple-layer pattern of SiO2, Si3N4, SiO2 and then executing thermal oxidation thereto.
CONSTITUTION: An SiO2 22, and Si3N4 23 by CVD method, SiO2 24 are laminated on the P type Si substrate 21. After a resist mask 25 is provided and these are sequentially etched, the surface is covered with Si3N4 29 using the SiH4+**NH3** gas. Thereafter, Si3N4 29 is left at side surface of; the Si3N4 27, SiO2 28 and a wall 30 is formed using the **CF4**+O2 gas by the reactive ion etching method. After providing a channel stop by injecting P ion, a field **oxide film** 31 is formed by heat treatment and the films 27, 28 30 are removed. An MOSFET is formed as specified in the element region by the ordinary method. According to this structure, the Si3N4 pattern 27 is protected by the SiO2 pattern 26, pin holes are not generated on the film 27 at the time of RIE processing, islands of SiO2 are not generated in the element forming region. Moreover, a bird beak is also rejected by the wall 30 and thereby integration density can be improved.

L4 ANSWER 51 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1984-055033 JAPIO
TI FORMATION OF INTERELEMENT ISOLATING FILM
IN SHIOTANI YOSHIMI
PA FUJITSU LTD, JP (CO 000522)
PI JP 59055033 A 19840329 Showa
AI JP1982-165740 (JP57165740 Showa) 19820922
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 255, Vol. 8, No. 1491, P. 99 (19840712)

AB PURPOSE: To enable to form the **insulating film** for interelement isolation with a small area by a method wherein after silicon nitride films are formed on the surfaces of phosphosilicate glass buried in etched grooves formed to a silicon substrate, a remaining SiO2 film on the surface of the substrate is removed.
CONSTITUTION: A PSG film 14 formed at the part other than the upper parts of the V-shaped grooves 12 is removed according to reactive ion etching using **CF4** gas and using a photo resist film patterned on the Si substrate 11 as the mask. Then after a photo resist film is formed on the substrate 11 excluding the parts of the PSG films 14 buried in the V-shaped grooves 12, the silicon nitride films 15 are formed on the PSG films 14 of the V-shaped grooves 12 using **ammonia** gas and silicon dichloride gas according to the CVD method. After then, photo resist films are formed again by patterning only on the PSG films 14 of the V-shaped grooves 12, and the silicon nitride films are removed according to dry etching using carbon tetrafluoride gas and oxygen. Accordingly the interelement isolating films consisting of the PSG film 14 the surface thereof being surrounded with the Si3N4 film and the sides and the base thereof being surrounded with the SiO2 film 13 can be formed.

L4 ANSWER 52 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1983-188141 JAPIO
TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN FUNADA ATSUSHI
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 58188141 A 19831102 Showa
AI JP1982-73153 (JP57073153 Showa) 19820427
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 225, Vol. 8, No. 251, P. 133 (19840202)
AB PURPOSE: To manufacture a semiconductor device with high reliability and high speed operability by a method wherein the **insulating films** between **layers** are divided into two or more layers and the first layer is grown in the vapor phase during glow discharge while the second layer is laminated by means of ordinary vapor growth preventing a hillock growth from happening.
CONSTITUTION: SiO2 film 12 on a substrate 11 is formed into a hole 19 to form Al thin film wiring 13 making **NH3** and SiH4 react during glow discharge to form Si3N4 film 20. At this time, the temperature of the substrate 11 may be sufficient at 200-300.degree.C preventing a hillock from happening. Firstly SiH4 and O2 are reacted to form SiO2 film 15 at the same evacuated condition. At this time, no hillock happens on the Al wiring 13 though it is exposed to the temperature at 400-500.degree.C as it is already covered with Si3N4 film 20. The SiO2 film 15 is selectively formed into a hole using HF solution and then the Si3N4 film 20 is formed into another hole 17 using **CF4** plasma. Secondly Al is evaporated to form another wiring 16. In this constitution, any defective withstand voltage between the wirings 13 and 16 may be reduced subject to less parasitic capacity preventing an abnormal reaction of the lower layer wiring 13 in case of forming another hole 17.

L4 ANSWER 53 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1983-093235 JAPIO
TI PREPARATION OF SEMICONDUCTOR DEVICE
IN HAZUKI RIYOUICHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 58093235 A 19830602 Showa
AI JP1981-190609 (JP56190609 Showa) 19811130
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 194, Vol. 7, No. 19, P. 94 (19830819)

AB PURPOSE: To electrically stabilize by removing the surface layer for the specified amount or more by the dry etching using plasma of F or the etching of solution containing HF, after removing **insulating film** surface **layer** by the reactive ion etching method.
CONSTITUTION: A field **oxide film** 2, gate **oxide film** 3 and poly Si gate electrode 4 are formed on a p type Si substrate 1, an n+ layers 5, 6 are formed by doping As, it is then covered with a CVD SiO2 7, thereafter an Si2N4 8 is stacked by the plasma CVD method using SiH4 and **NH3** are used. When the Si3N4 8 and SiO2 7 are partly removed by selecting the condition that the etching rates of SiO2 and Si3N4 becomes equal, using the reactive ion etching method with **CF4** and H2, a damage layer 9 is generated at the surface of remaining film 7. In succession, the damage layer 9 resulting from electrical unstability is removed for 100.ANG. or more by plasma due to a high-frequency discharge of CH4 and O2, for example. Moreover, a window is opened on the layer 7 and an electrode 10 is sttached. According to this constitution electrically stable flat **insulating film** can be obtained and a high reliably device can be obtained.

L4 ANSWER 54 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1982-211734 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN HAZUKI RIYOUICHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 57211734 A 19821225 Showa
AI JP1981-97699 (JP56097699 Showa) 19810624
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 165, Vol. 7, No. 651, P. 73 (19830318)
AB PURPOSE: To obtain an **insulating film** with an approximately flat surface with less influence by unevenness, by simultaneously performing anisotropic dry- etching, when vapor-growing an **insulating film** on the uneven surface.
CONSTITUTION: An SiO2 layer 2 and Al wiring 3 are formed on the substrate 1 and, when vapor-growing Si3N4 4 thereon, SiH4, and **NH3** as generation gases simultaneously with **CF4** as etching gas are added. In case of etching the **insulating film** by anisotropic etching, the etching speed for a convex region becomes higher than that for a concave region of the **insulating film** for rapid growth for the **insulating layer** of the concave region, finally obtaining an **insulating layer** with a smooth surface. The drawing represents the embodiment with the Al film thickness of approx. 1.mu.m, wiring width of approx. 2.mu.m and interval of an adjacent wiring of approx. 3.mu.m.

L4 ANSWER 55 OF 55 JAPIO COPYRIGHT 2002 JPO
AN 1982-075429 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN SHIMA SHOHEI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 57075429 A 19820512 Showa
AI JP1980-150991 (JP55150991 Showa) 19801028
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 124, Vol. 6, No. 1511, P. 154 (19820811)
AB PURPOSE: To form taper of 60-80.degree. on the side of an **insulating film** of semiconductor device and to prevent disconnection of a wiring layer at the step part by a method wherein a resist mask is applied on an Si3N4 film, and reactive ion etching is performed using a halogen compound of C containing H.
CONSTITUTION: The SiO2 film 23 is provided on an Si substrate 21 being

formed with an active layer 22, and the Si3N4 film 24 is accumulated thereon by the plasma CVD method using SiH4 and **NH3**. A resist mask 25 is applied thereon, and when the Si3N4 film 24 is etched by the reactive ion etching method of confronting electrodes structure making **CF4**+H2 to flow, taper of 60-70.degree. is formed at the side of an opening 26. The resist mask 25 is removed, and moreover when etching is performed in mixed gas of **CF4**+H2, an opening 26 having taper is formed also at the side of the SiO2 film 23. The remained Si3N4 film 24 can be eliminated in accordance with the etching condition. Because taper is formed on the side of the opening, disconnection of the Al wiring layer 27 is not generated.

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      FILE 'HCAPLUS' ENTERED AT 10:59:06 ON 24 MAY 2002
L1         13575 S FLUOROCARBON

      FILE 'REGISTRY' ENTERED AT 11:00:13 ON 24 MAY 2002
L2            35 S H3N/MF

      FILE 'HCAPLUS' ENTERED AT 11:00:28 ON 24 MAY 2002
L3           232 S L1 AND (NH3 OR L2 OR AMMONIA)
L4             8 S L3 AND (DIELECTRIC OR INSULAT? OR OXIDE)(3N)(LAYER OR FILM OR
```

=> D BIB AB 1-8

L4 ANSWER 1 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:837275 HCAPLUS
DN 134:35845
TI Fabrication of semiconductor devices by anisotropic etching of interlayer **insulator films**
IN Miyata, Koji
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 2000331992 | A2 | 20001130 | JP 1999-138302 | 19990519 |

AB The title fabrication involves anisotropic plasma etching of an interlayer **insulator film** employing a **fluorocarbon** and SOG mixt. contg. halo, Si, C, and O at a spec. desired ratio with an etchant contg. CO, H, N, **NH3**, water, and/or rare gases without use of **fluorocarbon** gases. The insulator materials and the etchant compn. give the etching of the **insulator film** without deterioration of the film quality.

L4 ANSWER 2 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:457321 HCAPLUS
DN 133:67307
TI Method of plasma etching silica using hydrogen-containing additive gases in **fluorocarbon** gas chemistry
IN Hills, Graham; Nguyen, Thomas; Keil, Douglas; Khajehnouri, Keyvan
PA Lam Research Corp., USA
SO PCT Int. Appl., 26 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI WO 2000039846 | A1 | 20000706 | WO 1999-US31077 | 19991228 |
| W: IL, JP, KR, SG | | | | |
| RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE | | | | |
| US 6217786 | B1 | 20010417 | US 1998-223963 | 19981231 |
| EP 1147549 | A1 | 20011024 | EP 1999-968192 | 19991228 |
| R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI | | | | |
| PRAI US 1998-223963 | A | 19981231 | | |
| WO 1999-US31077 | W | 19991228 | | |

AB A method of etching an **oxide layer** in a plasma etching reactor is disclosed. The method includes the steps of providing a semiconductor substrate including the **oxide layer** into the plasma etching reactor and flowing an etching gas that includes a **fluorocarbon** gas, a N reactant gas, an O reactant gas, an inert carrier gas, and a H-contg. additive gas into the plasma etching reactor. The method further includes etching an opening at least partially through the **oxide layer** using a plasma that is formed from the etching gas.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L4 ANSWER 3 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:13776 HCAPLUS
DN 128:69683
TI Etching a **dielectric layer** using a plasma generated from a mixture of **fluorocarbon** gas, **NH3**-generating gas, and a carbon-oxygen-containing gas
IN Ding, Ji; Shan, Hongching; Welch, Michael
PA Applied Materials, Inc., USA
SO Eur. Pat. Appl., 16 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 3

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | EP 813233 | A2 | 19971217 | EP 1997-304035 | 19970610 |
| | EP 813233 | A3 | 19990825 | | |
| | R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI | | | | |
| | US 5814563 | A | 19980929 | US 1996-660966 | 19960612 |
| PRAI | US 1996-660966 | | 19960612 | | |
| | US 1996-639388 | | 19960429 | | |

AB A method of etching a **dielec. layer** on a substrate with high selectivity, low etch rate microloading, and high etch rates is described. A substrate having a **dielec. layer** with resist material on it is placed in a process zone, a process gas is introduced into the process zone, and a plasma is formed from the process gas to etch the **dielec. layer** on the substrate. The process gas comprises (i) **fluorocarbon** gas for forming F-contg. etchant species capable of etching the **dielec. layer**; (ii) **NH3**-generating gas having a liquefaction temp. of .apprx.-60.degree. to .apprx.20.degree., and (iii) oxycarbon gas contg. C and O bonded to each other. The temp. of the substrate is maintained within about .+-.50.degree. of the liquefaction temp. of the **NH3** -generating gas.

L4 ANSWER 4 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:612484 HCAPLUS
DN 125:236273
TI Manufacture of semiconductor device with contact plug in interlayer **insulating layer**
IN Tamya, Naomiki
PA Sony Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 08203871 | A2 | 19960809 | JP 1995-9284 | 19950124 |

AB The method for forming a plug which fills a contact-hole involves the following steps: (1) opening a contact-hole in an **insulator film**, (2) forming a conductive layer on the whole surface of the **insulator film** so that the conductive layer enters the contact-hole, and (3) etching the conductive layer by using an etching gas

to leave part of the conductive layer only in the contact-hole. The etching gas used in the step 3 contains a certain gas, which may be H, HCl, **NH3**, HBr, or **fluorocarbon** (CHF3, CH2F2, CH3F, or CH4). In the method, radicals are formed in the step 3, and the radicals react with the conductive layer and etch the conductive layer. The excess radicals are scavenged by that gas in the etching gas.

L4 ANSWER 5 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1984:130915 HCAPLUS
DN 100:130915
TI Insulation of semiconductor wiring
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 58197822 | A2 | 19831117 | JP 1982-79961 | 19820514 |

AB Interlayer insulation of Al wirings on semiconductor devices is achieved without disconnections by depositing a thin Si3N4 film over the 1st Al layer by a combined discharge and reactive sputter etching in a gas contg. SiH4, N2, **NH3**, and a sputter etchant such as CF4 to form smooth steps, and depositing the 2nd Al film.

L4 ANSWER 6 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1983:585912 HCAPLUS
DN 99:185912
TI Semiconductor devices with electrically stable **insulator films**
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| JP 58093235 | A2 | 19830602 | JP 1981-190609 | 19811130 |

AB The elec. stability of SiO2 **insulator films** is greatly increased by dry etching it in a F plasma or an etchant contg. HF after it has been reactive-ion etched with CF4 and H2 during device fabrication. Thus, SiO2 field and gate **oxide films** were formed on p-Si contg. As-doped n+ layers, SiO2 and Si3N4 (from SiH4-**NH3** plasma) films were deposited, the SiO2 and Si3N4 layers were partially etched with a CF4-H2 mixt., the damage layer was etched off in a CF4-O2 plasma, windows were opened, and the electrodes formed.

L4 ANSWER 7 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1975:611326 HCAPLUS
DN 83:211326
TI Oleophobic compositions of fluorinated polymers and oils for lithographic plates
IN Yoerger, William E.; McCabe, John M.; Wright, John F.
PA Eastman Kodak Co., USA
SO U.S., 14 pp. Division of U.S. 3,859,090.
CODEN: USXXAM
DT Patent

LA English
FAN.CNT 3

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 3901700 | A | 19750826 | US 1974-497348 | 19740813 |
| | US 3859090 | A | 19750107 | US 1973-361370 | 19730517 |
| | US 3975352 | A | 19760817 | US 1975-558030 | 19750313 |
| PRAI | US 1973-361370 | | 19730517 | | |
| | US 1974-497348 | | 19740813 | | |

AB Oleophobic coating compns. for lithog. plates are comprised of a low-volatility oil having a surface energy <27 dyne/cm, such as fluorinated oils and polysiloxane oils, a solid fluorinated polymer having a F content of .gtoreq.40% based on a total mol. wt. of the polymer, such as 1,1-dihydroperfluorobutyl acrylate polymer, and a hydrophobic resinous binder, esp. fluorinated hydrocarbon resins and silicone resins. The compns. provide coatings that are less subject to abrasion as well as contamination and smudging by planog. developer app. and by developer and ink compns. Also, they are suitable for use in an electrog. app. for the prepn. of these plates. Thus, an elec. conducting support was **coated** with an elec. **insulating layer** of Gelva C5-V16 poly(vinyl acetate) resin, treated with a slightly alk. (**ammonia**) aq. soln. contg. 20 wt.% solids, overcoated at 0.001 in. wet thickness with a soln. contg. 2 wt.% solids comprised of Kel F-800 vinylidene fluoride-trifluorochloroethylene polymer 64, TLF2916 fluoropolymer 16, and Krytox 143AC perfluoroalkyl polyether oil 20 wt.%, cured at 125.degree.F for 1 min, an electrostatic charge pattern formed on its surface, developed with an electrog. developer contg. oleophilic toner particles, the toner image fused to the surface of the coating compn., and the resultant plate used to prep. a multiple no. of copies, the ink used being G.P.I. Dri Lith Ink contg. an Al isopropoxide additive.

L4 ANSWER 8 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1958:112883 HCAPLUS
DN 52:112883
OREF 52:19879b-c
TI Depassifying high-chromium steels prior to nitriding
IN Low, Sidney
PA Chapman Valve Manufg. Co.
DT Patent
LA Unavailable
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 2851387 | | 19580909 | US | |

AB An inert or passive **oxide film** of Cr **oxide** on these steels is a hindrance to nitriding. The oxide may be removed by the gaseous decompn. product of a **fluorocarbon**. Samples of type-304 and -410 stainless steel were heated in a nitriding furnace along with pieces of **fluorocarbon** at 900.degree.F. **NH3**, dissocd. 5-20%, was circulated into the retort. The type-304 sample, after cooling, tested 88.5 Rockwell N after treatment, and 77 before. The case depth was 0.003 in. The type-410 sample tested 91.5 Rockwell N after nitriding, as compared to 77 before. The case depth was 0.0045 in. The time of treatment may vary from a few min. to 100 hrs.

File 2:INSPEC 1969-2002/May W3


| Set | Items | Description |
|---|---|---|
| S1 | 11 | CI=C4F8 BIN |
| S2 | 0 | CI=C4F6 BIN |
| S3 | 0 | CI=C5F8 BIN |
| S4 | 98 | CI=CF4 BIN |
| S5 | 15 | CI=C2F6 BIN |
| S6 | 4 | CI=C3F8 BIN |
| S7 | 5152 | CI=NH3 BIN |
| S8 | 1569 | FLUOROCARBON OR (CARBON ()FLUORIDE) |
| S9 | 11976 | AMMONIA (January 1969) |
| S10 | 32052 | (DIELECTRIC OR INSULAT? OR OXIDE)(3N)(LAYER OR FILM OR COAT????) |
| S11 | 119 | S1:S6 |
| S12 | 1 | S11 AND (S7 OR S9) |
| S13 | 0 | S1 AND (S7 OR S9) |
| S14 | 0 | S2 AND (S7 OR S9) |
| S15 | 1 | S4 AND (S7 OR S9) |
| S16 | 0 | S5 AND (S7 OR S9) |
| S17 | 0 | S6 AND (S7 OR S9) |
| S18 | 3 | S8 AND (S7 OR S9) |
| S19 | 3 | S18 NOT S12 |
| S20 | 31 | (C4F8 OR C4F6 OR C5F8 OR CF4 OR C2F6 OR C3F8) |
| S21 | 0 | S20 AND (S7 OR S9) |

12/3,AB/1
DIALOG(R)File 2:INSPEC


03536211 INSPEC Abstract Number: B90007792
Title: Fabrication of amorphous silicon photoreceptor. I. Kinetics of glow-discharge decomposition of SiH/sub 4/ and related reactive gases
Author(s): Nakanishi, T.; Marukawa, Y.; Takahashi, S.; Yamazaki, T.; Moriguchi, H.
Author Affiliation: Konica Corp., Tokyo, Japan
Journal: Electrophotography vol.28, no.3 p.274-83
Publication Date: 1989 Country of Publication: Japan
CODEN: ELPYAW ISSN: 0387-916X
Language: English
Abstract: Decomposition efficiencies ( eta ) of SiH/sub 4/ and the related source gases X have been measured by mass spectrometry in SiH/sub 4/-X-Ar glow-discharge plasma, and the relative rate constants for dissociation reaction of the gases X to SiH/sub 4/ (K/sub d,X//K/sub d,SiH4/) have been determined, where X are Si/sub 2/H/sub 6/, GeH/sub 4/, C/sub 2/H/sub 2/, NH/sub 3/, CH/sub 4/, CO/sub 2/, CF/sub 4/, and SiF/sub 4/. Using these kinetic data obtained, incorporation process of carbon-source species into a-SiC:H films and resultant carbon contents (C) in the films have been discussed for SiH/sub 4/, CH/sub 4/ and C/sub 2/H/sub 2/ as material gases. Furthermore, a-Si:H/a-SiC:H double-layer-red photoreceptors have been fabricated under controlling eta /sub SiH4/ and eta /sub CH4/ in SiH/sub 4/-CH/sub 4/-Ar glow-discharge plasma and their electrophotographic properties have been presented.
Subfile: B

19/3,AB/1
DIALOG(R)File 2:INSPEC


6477650 INSPEC Abstract Number: B2000-03-2550G-017
Title: Novel approach for the photostabilization of chemically amplified photoresists
Author(s): Carpio, R.A.; Martinez, R.A.; Mohondro, R.D.
Author Affiliation: SEMATECH, Austin, TX, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3678, pt.1-2 p.935-46
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3678:1/2L.935:NAPC;1-0
Material Identity Number: C574-1999-215
U.S. Copyright Clearance Center Code: 0277-786X/99/$10.00
Conference Title: Advances in Resist Technology and Processing XVI
Conference Sponsor: SPIE
Conference Date: 15-17 March 1999 Conference Location: Santa Clara, CA, USA
Language: English
Abstract: A special UV curing process which employs an **ammonia** blanketing gas was investigated to determine if a reduction in chemically amplified photoresist loss cold be attained in oxide, polysilicon, and metal plasma etch processes. In addition, a reduction in film shrinkage was sought relative to curing processes, which do not employ a basic gas during the stabilization process. Representative commercially available 248 nm chemically amplified photoresists from the t-BOC, acetal, and ESCAP families were included in this study. These studies were limited to unpatterned resist films and were conducted with an H-mod bulb, having a wavelength cut-off of 250 nm. The parameters varied in this study included UV irradiation intensity, process time, and temperature. Film shrinkage, refractive index, FTIR spectral changes, dissolution properties in an alkaline developer, and etch rate properties in **fluorocarbon** and chlorine based plasmas were measured. It was demonstrated that the **ammonia** -based photostabilization process result in less film shrinkage than the corresponding process with no basic purge gas. Evidence is provided that cross linking result from the UV curing process. The photostabilization process has been optimized for a number of photoresists to minimize the film shrinkage resulting from photostabilization and to significantly reduce the plasma etch rate. Benefits are shown to be greater for low activation energy and t-BOC type resists.
Subfile: B


19/3,AB/2
DIALOG(R)File 2:INSPEC


5354485 INSPEC Abstract Number: A9619-8265-013
Title: Surface modification of **fluorocarbon** polymers by vacuum-UV excimer lamp irradiation in reactive gas atmosphere
Author(s): Heitz, J.; Niino, H.; Yabe, A.
Author Affiliation: Nat. Inst. of Mater. & Chem. Res., Ibaraki, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers,

Short Notes & Review Papers) vol.35, no.7 p.4110-16
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: July 1996 Country of Publication: Japan
ISSN: 0021-4922
SICI: 0021-4922(199607)35:7L.4110:SMFP;1-8
Material Identity Number: F221-96005
Language: English
Abstract: Irradiation of poly(tetrafluoroethylene) (PTFE) and poly(tetrafluoroethylene-co-hexafluoropropylene) (FEP) polymer films in an **ammonia** or hydrazine atmosphere with vacuum UV light resulted in a hydrophilic surface, where abstraction of fluorine atoms and introduction of nitrogen, oxygen, and hydrogen atoms occurred. We used Kr/sub 2/* and Xe/sub 2/* excimer lamps at wavelengths of 172 nm and 146 nm, respectively. The reaction mechanism for chemical surface modification is discussed on the basis of the results of X-ray photoelectron spectroscopy, secondary ion mass spectrometry, scanning electron spectroscopy, and attenuated total reflection Fourier transform infrared spectroscopy analyses.
Subfile: A


19/3,AB/3
DIALOG(R)File 2:INSPEC


01913844 INSPEC Abstract Number: A82088241, B82045964
Title: Reactive ion etching of silicon oxides with **ammonia** and trifluoromethane. The role of nitrogen in the discharge
Author(s): Smolinsky, G.; Truesdale, E.A.; Wang, D.N.K.; Maydan, D.
Author Affiliation: Bell Labs., Murray Hill, NJ, USA
Journal: Journal of the Electrochemical Society vol.129, no.5 p. 1036-9
Publication Date: May 1982 Country of Publication: USA
CODEN: JESOAN ISSN: 0013-4651
Language: English
Abstract: A 4% NH/sub 3//CHF/sub 3/, RIE discharge accurately reproduced micron-sized features in SiO/sub 2//Si or P-glass/Si substrates which had been patterned with either photoresist or X-ray trilevel resist. Etch rates of up to 600 and 1200 AA/min were obtained with SiO/sub 2/ and P-glass, respectively; etch rate ratios for SiO/sub 2//Si and P-glass/Si were approximately 15 and 30, respectively. Erosion of the resist was slow enough that it did not interfere with pattern transfer. In addition, no undercutting occurred and sidewalls in etched features were nearly vertical. **Ammonia** inhibited **fluorocarbon** polymer deposition by reaction with any deposit formed to make volatile cyanogen derivatives. Moreover, NH/sub 3/ moderated deterioration of the resist by the plasma.
Subfile: A B